# Capacitive Power Transfer for Contactless Charging

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***Abstract*— The simplicity and low cost of capacitive interfaces makes them very attractive for wireless charging stations. Major benefits include low electromagnetic radiation and the amenability of combined power and data transfer over the same interface.**

**We present a capacitive power transfer circuit using series resonance that enables efficient high frequency, moderate voltage operation through soft-switching. An included analysis predicts fundamental limitations on the maximum achievable efficiency for a given amount of coupling capacitance and is used to find the optimum circuit component values and operating point. Automatic tuning loops ensure the circuit operates at the optimum frequency and maximum efficiency over a wide range of coupling capacitance and load conditions.**

**An example interface achieves near 80% efficiency at 3.7 W with only 63 pF of coupling capacitance. An automatic tuning loop adjusts the frequency from 4.2 MHz down to 4 MHz to allow for 25% variation in the nominal coupling capacitance. The duty cycle is also automatically adjusted to maintain over 70% efficiency for light loads down to 0.3 W.**

## I. Introduction

Wireless power delivery is gaining increasing attention for powering and charging portable devices including smart phones, cameras, and laptop computers. The predominant solution today uses an inductive [1], [2] interface between a charging station, acting as the transmitter, and a receiver, typically a portable device. Both the transmitter and receiver are fitted with electrical coils. When brought into physical proximity, power flows from the transmitter to the receiver. Here we examine an alternative approach that uses a capacitive, rather than inductive interface to deliver power—Fig. 1. In the capacitive interface the field is confined between conductive plates, alleviating the need for magnetic flux guiding and shielding components that add bulk and cost to inductive solutions [3].

The realizable amount of coupling capacitance is limited by the available area of the device, imposing a challenging design constraint on contactless power delivery. The parallel plate capacitance across a 1/4 mm air gap is only 3.5 pF/cm$^2$, limiting typical interface capacitance to a few tens of picofarads, and the required charging power is upwards of 2.5 W (USB-specification). Existing capacitive power transfer (CPT) solutions either use much larger capacitors [4] or are targeted at lower power applications, such as coupling of power and data between integrated circuits [5] or transmitting power and data to biosignal instrumentation systems [6], [7]. This work presents a design methodology that results in a circuit that uses the available capacitance as efficiently as possible, exposing a fundamental trade-off between the available coupling capacitance and maximum obtainable efficiency for a desired output power.

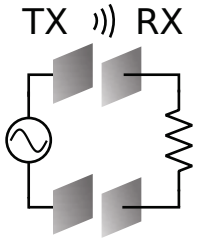


Fig. 1. Power is transferred from an AC source to a load through capacitors formed by parallel plates on a transmitter and a receiver.

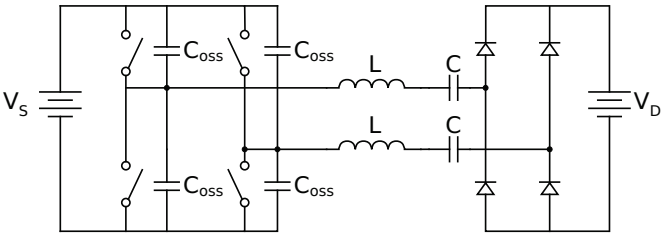


Fig. 2. Schematic of a series resonant converter circuit constructed around the coupling capacitors $C$.

Section II presents the analysis of the CPT circuit, including an efficiency expression that accounts for all relevant loss mechanisms. Section III discusses how to design a circuit given the results of the analysis. Section IV presents experimental results from an example design suitable for USB-level power delivery in a smartphone sized package.

## II. Analysis

The analysis is based on a series resonant architecture, presented in Fig. 2. Power is transferred from $V_S$ to $V_D$ through the two coupling capacitors $C$. These two capacitors are in series, so the effective capacitance between transmitter and receiver is $C/2$. An H-bridge driver converts $V_S$ into an AC voltage to enable current flow through the capacitors. Inductors $L$ are placed in series with the coupling capacitance to reduce the impedance between the transmitter and receiver at resonance and to enable soft-switching. A diode rectifier converts the AC voltage back to DC. A voltage source models the load, which is equivalent to a resistive load in parallel with a sufficiently large hold-up capacitor.

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Similar architectures appear in [8] and [9] with the differences being unbalanced operation and use of an additional frequency selective tank. A differential driver reduces EMI by suppressing the common mode signal on the receiver. Eliminating the additional tank permits dynamically tuning the frequency to adapt to a variable coupling capacitance.

The switches used in the H-bridge have three relevant parasitics: the on-resistance $R_{on}$, the drain capacitance $C_{oss}$, and the gate capacitance $C_g$. The technology-dependent parameter $\tau_{sw}$ is used to model the sizing trade-off between on-resistance and drain capacitance as $R_{on} = \tau_{sw}/C_{oss}$. If hard-switched, the parasitic $C_{oss}$ capacitors cause $4C_{oss}V_S^2 f$ switching loss, where $f$ is the operating frequency. This loss can be eliminated by operating the circuit in a zero voltage switching (ZVS) regime, where the inductor recovers the charge on the $C_{oss}$ capacitors, and no current impulses are drawn through the switches. Similarly, the loss from driving the gates is $4C_g V_G^2 f$, where $V_G$ is the gate drive voltage. In practical CPT designs for contactless charging, $V_D$ is much greater than $V_G$, so the drain capacitance loss term dominates. The gate loss is not considered in the analysis for clarity, but it is not conceptually difficult to include.

The series resonant architecture has been extensively analyzed in [10]–[12]. The following analysis differs in that the coupling capacitance, $C$, is treated as the scarce parameter. The goal is to determine a circuit design that uses the available $C$ as efficiently as possible. The input parameters are the output power, $P_{out}$, the source voltage, $V_S$, and the technology-dependent parameters $Q$ and $\tau_{sw}$. The analysis determines the relationship between the available coupling capacitance and the *maximum* achievable efficiency. From this, we can design a circuit that requires the least amount of coupling capacitance to achieve the efficiency $\eta$. The switch size parameter is captured by $C_{oss}$. It is convenient to require $Q$ as an input, as it accurately models the inductor loss and is generally well-known for a particular inductor technology.

### A. Efficiency

The efficiency of the converter considering the conduction losses only is given by

$$\eta = 1 - \frac{1}{2}\frac{||i_t||^2 R_S}{P_{out}}, \tag{1}$$

where $||i_t||$ is the magnitude of the tank current and $R_S$ is the effective parasitic series resistance due to the inductor, capacitor, and switch. The tank current, $i_t$, is assumed to be sinusoidal due to the frequency selectivity of the tank; thus, the standard definitions of magnitude and phase apply. Typically, the inductor will have a much lower $Q$ than the capacitor, so $R_S$ can be approximated by

$$R_S \approx 2\left(R_{on} + \frac{\omega L}{Q}\right), \tag{2}$$

where $\omega = 2\pi f$ and the factor of 2 is from the series combination of switches and inductors. Substituting (2) into (1) and using the $\tau_{sw}$ parameter, the efficiency expression becomes

$$\eta = 1 - \frac{||i_t||^2(\tau_{sw}/C_{oss} + \omega L/Q)}{P_{out}}. \tag{3}$$

Currently, the problem is underconstrained. To proceed, $||i_t||$ should be expressed as a function of $C$, and the ZVS condition should be enforced.

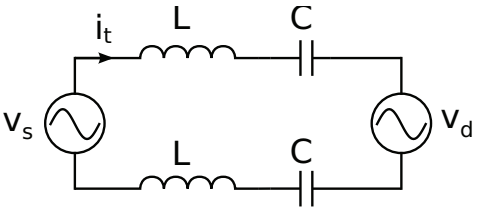


Fig. 3. Circuit used for calculating the tank current as a function of the applied phasor voltages.

### B. Tank Current

The circuit in Fig. 3 is used to derive the tank current, $i_t$, using phasor analysis and neglecting harmonics. The voltage sources $v_s = V_S\angle 0$ and $v_d = V_D\angle\phi$ are applied to the series resonant circuit. Since the (ideal) rectifier in Fig. 2 can only consume power, $i_t$ is restricted to be in phase with $v_d$. This is equivalent to assuming that the diodes have no parasitic capacitance. Then the phase shift is given by

$$\phi = \angle\left(\frac{i_t}{v_s}\right) = \arctan\left(-\sqrt{\frac{V_S^2}{V_D^2} - 1}\right). \tag{4}$$

The magnitude of the current is given by

$$||i_t|| = \frac{1}{2}\frac{Q\omega_0 C}{Q(\frac{\omega}{\omega_0} - \frac{\omega_0}{\omega}) + 1}\sqrt{V_S^2 - V_D^2}, \tag{5}$$

where $\omega_0 = 1/\sqrt{LC}$ is the resonant frequency and $\omega$ is the applied frequency. For high unloaded $Q$, this can be approximated by

$$||i_t|| \approx \frac{1}{2}\frac{\omega C}{\omega^2 LC - 1}\sqrt{V_S^2 - V_D^2}. \tag{6}$$

### C. Zero Voltage Switching Condition

Since the efficiency expression considers only conduction losses due to switch and inductor resistance, a ZVS condition should be enforced to validate the analysis. ZVS occurs when the tank current fully commutates the $C_{oss}$ capacitors during the time when all switches in the H-bridge are open. This time interval is known as the dead-time of the driver. The initial and desired final states of the $C_{oss}$ capacitors are known; two start at $V_S$ and must be discharged to zero volts, and two are initially at zero volts and must be charged to $V_S$.

Consider the $C_{oss}$ capacitors initially charged to $V_S$; together they store $q_{sw} = 2C_{oss}V_S$ charge. This is the amount of charge that the tank current must displace during the dead-time interval to satisfy ZVS. Since the magnitude of $i_t$ is known, the maximum possible charge that the tank can remove from the capacitor can be calculated by integrating the portion

of $i_t$ corresponding to discharging $C_{oss}$. The time interval to be integrated is from the falling edge of the H-bridge output voltage to the zero crossing of the tank current. Immediately before this time interval, the H-bridge is still driving the output, so the tank current is sourced from $V_S$, not $C_{oss}$. After this time interval, the current changes direction, thus is flowing in a direction to charge, rather than discharge $C_{oss}$. Fig. 5 represents this graphically.

The time interval just described simply corresponds to the phase shift between the H-bridge output voltage and the tank current, which has already been calculated as $\phi$ above. Using a cosine reference for the phasor $i_t$,

$$i_t = ||i_t|| \cos(\omega t + \phi), \tag{7}$$

the integral that gives the average value of the current is

$$I_{avg} = -\frac{1}{\phi}\int_{\pi/2+\phi}^{\pi/2} ||i_t|| \cos\theta d\theta = -\frac{||i_t||}{\phi}(1-\cos\phi), \tag{8}$$

where $\phi$ is negative (current lags voltage), making the result positive. Multiplying by the integration time gives

$$q_t = \frac{||i_t||}{\omega}(1-\cos\phi), \tag{9}$$

where $q_t$ represents the maximum amount of charge that the tank can displace. The ZVS condition is then $q_t \geq q_{sw}$ or

$$\omega \leq \frac{||i_t||}{V_S 2C_{oss}}(1-\cos\phi). \tag{10}$$

The output power and current are related by

$$P_{out} = 0.64||i_t||V_D, \tag{11}$$

where the constant 0.64 is from averaging a rectified sine wave, so (10) can be refactored as

$$\omega \leq \frac{P_{out}}{0.64 V_D V_S 2C_{oss}}(1-\frac{V_D}{V_S}) = \omega_{max}. \tag{12}$$

This result predicts that there is a maximum frequency beyond which ZVS does not occur.

### D. Minimum Capacitance

The capacitance is minimized with $\omega = \omega_{max}$, which can be seen by combining (6) and (11). The result is

$$C = \frac{1}{\omega\left(\omega L - 0.64 V_D \sqrt{V_S^2 - V_D^2}/(2P_{out})\right)}, \tag{13}$$

which is minimized for large $\omega$. Equations (13) and (2) with this choice of $\omega$ give

$$\begin{aligned} R_S = {} & 2R_{on} \\ & + 0.64\frac{2}{Q}\frac{V_D^2}{P_{out}} \\ & \times \left(\frac{2C_{oss}}{C}\frac{1}{A_V(1-A_V)} + \frac{1}{2}\sqrt{\frac{1}{A_V^2}-1}\right), \end{aligned} \tag{14}$$

where $A_V$ is the voltage conversion ratio $V_D/V_S$. Using (11) and (14), the efficiency as given in (3) can be expressed as

$$\begin{aligned} \eta = {} & 1 - \frac{P_{out}\tau_{sw}}{(0.64 A_V V_S)^2 C_{oss}} - \frac{1}{Q}\frac{1}{0.64} \\ & \times \left(\frac{2C_{oss}}{C}\frac{1}{A_V(1-A_V)} + \frac{1}{2}\sqrt{\frac{1}{A_V^2}-1}\right). \end{aligned} \tag{15}$$

The interpretation of this efficiency expression in terms of how it relates to circuit design is discussed in the next section.

## III. Design

The expression (15) contains two loss terms. The first is due to the switch on-resistance and the second to the inductive loss component. Assume the goal is to maximize the efficiency for a given coupling capacitance, $C$. If only the first term is considered, the switch size ($C_{oss}$), $V_S$, and $A_V$ should be as large as possible. If only the second term is considered, $Q$ should be maximized, the switch size minimized, and there is an optimum value for $A_V$. Since the two loss terms predict opposite impacts of $C_{oss}$, both should be considered to find the optimum switch size. It is always desirable to choose a switch with low $\tau_{sw}$ and an inductor with high $Q$ since this corresponds to a better switch or inductor, respectively. A high source voltage $V_S$ is desirable to reduce conduction losses but is often limited by practical constraints such as safety or compatibility with available step-down converters. The following example design demonstrates the utility of this equation.

### A. Example Design Process

A capacitive power transfer circuit is to be designed to meet USB-level power specifications, 2.5 W at 5 V. To meet these specifications, we first choose $V_S = 35\,\text{V}$, $P_{out} = 4\,\text{W}$, and $\tau_{sw} = 44\,\text{ps}$. The choice of $V_S$ is based on the decision to use a 60 V family of Siliconix switches as well as the convenience of a single-stage step-down to 5 V. $P_{out}$ is chosen conservatively to allow for some inefficiency of this final step-down. The $\tau_{sw}$ parameter is representative of the same family of Siliconix switches.

Fig. 4 is a plot of the maximum achievable efficiency as a function of the available coupling capacitance. Several values of the unloaded $Q$ are plotted to show the effect of the inductor loss. This plot was generated by substituting the above parameters into (15) and using numerical methods to find the maximum $\eta$ at each $C$. This maximum $\eta$ value corresponds to optimum values of $A_V$ and switch size ($C_{oss}$).

An alternative way to interpret this plot is that a target efficiency corresponds to a minimum required coupling capacitance. The capacitance must increase by nearly two orders of magnitude to increase the efficiency from 50% to 90%. Also, increasing the unloaded $Q$ by a factor of 2 reduces the required capacitance by approximately half.

As an example, we chose an operating point corresponding to $\eta = 0.9$ and $Q = 40$. The minimum $C$ is 147 pF, corresponding to $A_V$ and $C_{oss}$ (switch size) equal to 0.8 and 13 pF, respectively. Using these parameters and the results of

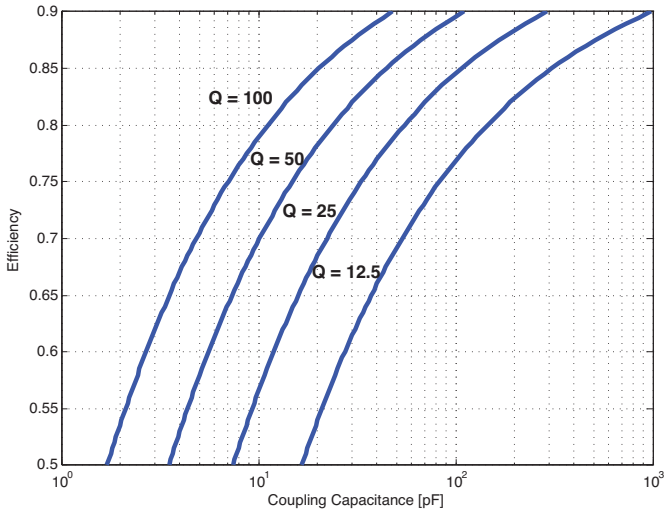


Fig. 4. Maximum achievable efficiency vs. available capacitance for several unloaded $Q$ values with $P_{out} = 4\,\mathrm{W}$, $V_S = 35\,\mathrm{V}$, and $\tau_{sw} = 44\,\mathrm{ps}$.

| Parameter | Expression | Value |
|---|---|---|
| $\omega$ | $\frac{P_{out}}{0.64 A_V V_S^2 2C_{oss}}(1 - A_V)$ | $2\pi 7.8\,\mathrm{Mrad/s}$ |
| $L$ | $\frac{1}{\omega^2 C}\left(\frac{0.64}{2}\frac{\omega C A_V V_S^2\sqrt{1-A_V^2}}{P_{out}} + 1\right)$ | $3.8\,\mu\mathrm{H}$ |
| $R_{on}$ | $\frac{\tau_{sw}}{C_{oss}}$ | $3.4\,\Omega$ |
| $V_D$ | $A_V V_S$ | $28\,\mathrm{V}$ |
| $\omega_0$ | $\frac{1}{\sqrt{LC}}$ | $2\pi 6.7\,\mathrm{Mrad/s}$ |
| $R_L$ | $\frac{2\times 0.64^2 V_D^2}{P_{out}}$ | $161\,\Omega$ |
| $Q_L$ | $\frac{2}{R_L}\sqrt{\frac{L}{C}}$ | 1.9 |
| $\|\|i_t\|\|$ | $\frac{P_{out}}{(0.64 V_D)}$ | $223\,\mathrm{mA}$ |
| $\phi$ | $\arctan\left(-\sqrt{\frac{1}{A_V^2} - 1}\right)$ | $-37°$ |
| $I_{out}$ | $\frac{P_{out}}{V_D}$ | $143\,\mathrm{mA}$ |

TABLE I

DESIGN EQUATIONS AND COMPONENT VALUES

the above analysis, the circuit design is complete. See Table I for all design equations and final component values. The parameters $R_L$, $Q_L$, and $I_{out}$ are the effective load resistance, the loaded Q, and the DC output current, respectively. This design is optimum in that it uses the smallest coupling capacitance possible to achieve the target specifications (equivalently, the maximum efficiency for this particular value of coupling capacitance).

| Parameter | Design | Simulation |
|---|---|---|
| $P_{out}$ | 4 W | 3.75 W |
| $\eta$ | 0.9 | 0.9 |
| $\|\|i_t\|\|$ | 223 mA | 196 mA |
| $I_{out}$ | 143 mA | 133 mA |

TABLE II

SIMULATION RESULTS

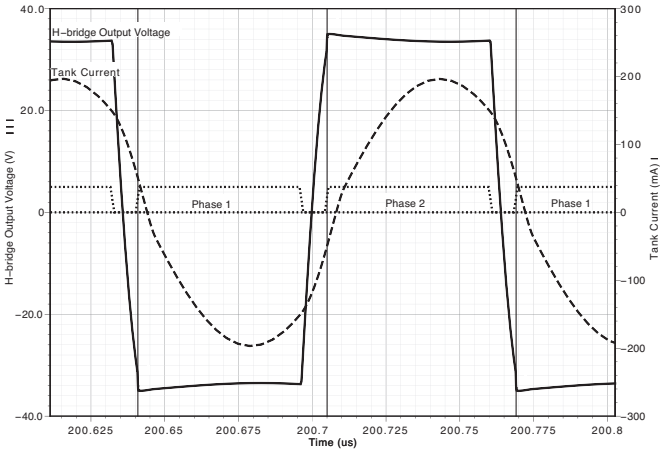


Fig. 5. Simulation results of example design showing ZVS. Solid: H-bridge output voltage. Dashed: Tank current. Dotted: Gate drive voltages.

### B. Simulation Results

The above design was simulated in Spectre. The results are summarized in Table II. Fig. 5 shows the waveforms of the H-bridge output voltage and tank current, along with the gate voltages which drive the H-bridge. The voltage is commutated by the tank current during the dead-time of the H-bridge, indicating that the design meets the ZVS condition. The next section presents experimental results that verify this design methodology.

## IV. USB-LEVEL CAPACITIVE POWER TRANSFER SYSTEM

This section presents the design and experimental verification of a 3.7 W, near 80% efficient CPT system requiring only 63 pF of series coupling capacitance, suitable for USB-level power delivery to a smartphone sized package. The design procedure in Section III is used to guide the design of the series resonant circuit. Techniques are presented that allow the circuit to remain near the optimum operating point as long as $C$ is larger than the minimum required coupling capacitance and $P_{out}$ is less than or equal to the design value. That is, the system is made tolerant to changes in alignment and load conditions. This is accomplished by automatically tuning the operating frequency and adjusting the duty cycle, respectively.

### A. Series Resonant Circuit Design

A slight modification to the methodology presented in Section III is made to account for the rectifier non-ideality. The rectifier has two parasitics: conduction loss and parasitic capacitance. Assume that parasitics are the same as those of the H-bridge by design. The conduction loss can be modeled

| Parameter | Design | Simulation | Experimental |
|---|---|---|---|
| $P_{out}$ | 4 W | 4 W | 3.72 W |
| $\eta$ | 0.8 | 0.81 | 0.77 |
| $\|\|i_t\|\|$ | 223 mA | 222 mA | — |
| $I_{out}$ | 143 mA | 142 mA | 133 mA |
| $\angle(v_d/v_s)$ | $-37°$ | $-32°$ | $-48°$ |

TABLE III

DESIGNED, SIMULATED, AND EXPERIMENTAL RESULTS

with either a voltage drop or equivalent on-resistance. This on-resistance has the same impact on the design equations as $R_{on}$. Parameter $\tau_{sw}$ is multiplied by 2 to account for this parasitic.

The parasitic capacitance creates an LCC resonant circuit that acts as an impedance transformation between the series tank and the rectifier input. The impedance seen by the tank is reduced, and there is voltage gain to the input of the rectifier. This implies that the voltage $v_d$ in Fig. 3 is increased, thus $i_t$ is reduced. The ZVS condition then becomes more strict according to (10). An exact analysis is not provided for the new condition, but this effect is mitigated by multiplying $\tau_{sw}$ by an additional factor of 2. This increases the $C_{oss}$ parameter in (10) and works well in practice.

The design presented in Section III was redone with $\tau_{sw} = 4\times44\,\text{ps}$ to account for the rectifier capacitance and conduction loss. We relaxed $\eta$ to 0.8 to reduce the required amount of capacitance. Using the above methods, the minimum $C$ is 125 pF, corresponding to $A_V = 0.8$, $L = 13.1\,\mu\text{H}$, $C_{oss} = (2)12\,\text{pF}$, $R_{on} = (2)3.5\,\Omega$, and $f = 4.2\,\text{MHz}$. Note that half of both $C_{oss}$ and $R_{on}$ is contributed by the H-bridge switch and half by the rectifier switch (diode).

The circuit was implemented with discrete components on a printed circuit board (PCB). The components were chosen to match the above design as closely as possible. The Siliconix 1029X Complementary N- and P-channel MOSFETs are chosen as the H-bridge switches. The specifications are $R_{on} = 5.5\,\Omega$ and $C_{oss} = 8\,\text{pF}$, so $\tau_{sw} = 44\,\text{ps}$, which is no coincidence. To be clear, the optimization done above would suggest that we increase the size of the switch such that $R_{on} = 3.5\,\Omega$ and $C_{oss} = 12\,\text{pF}$.

The rectifier is composed of NXP PMEG6002EJ Schottky diodes which have approximately the same capacitance and conduction loss as the switches. The inductor is a Coilcraft 1812LS, which is a surface-mount, ferrite-core part with $L = 12\,\mu\text{H}$ and $Q = 42$. The capacitive interface is implemented with PCB capacitors separated by a Kapton film dielectric and two layers of soldermask. The PCBs were clamped together to minimize capacitance variation due to imperfect flatness. The total gap is about 0.13 mm with a dielectric constant of 3. The plate area required is then calculated as $6\,\text{cm}^2$. The capacitance was adjusted through alignment to be 125 pF to make an accurate comparison between calculated, simulated, and experimental results.

The experimental setup is essentially identical to Fig. 2. The switching frequency was set to 4.2 MHz with 15 ns of dead-time between the clock phases. The load voltage was set to

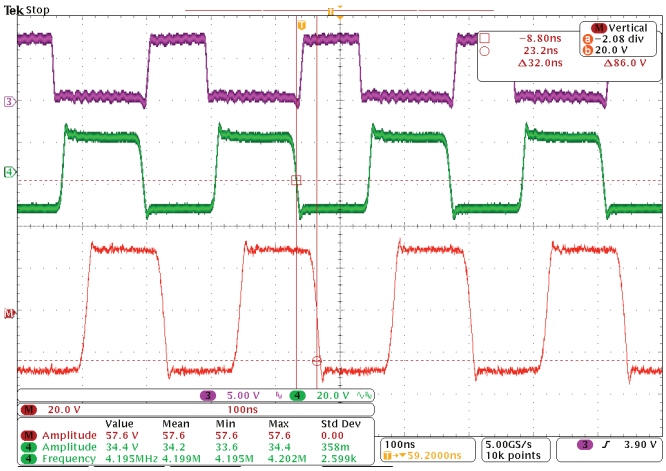


Fig. 6. Experimental results showing ZVS. Top: 1 phase of gate drive voltage (5 V/div). Middle: 1 phase of H-bridge output voltage (20 V/div). Bottom: Differential input voltage to rectifier (20 V/div). Time scale is 100 ns/div.

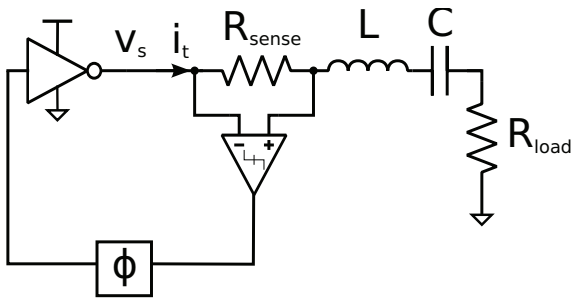


Fig. 7. Simplified schematic of automatic frequency tuning loop.

28 V. The input and output currents were measured to calculate the output power and efficiency. The results are included in Table III. An oscilloscope capture of the H-bridge drive waveform showing ZVS is given in Fig. 6. This figure also shows the differential input voltage to the rectifier, which lags the H-bridge voltage by 32 ns or 48°. The increase in phase shift from simulated to experimental results can be attributed to parasitic loading from the oscilloscope probes.

### B. Automatic Frequency Tuning

In order to make the performance of the powertrain insensitive to the exact amount of coupling capacitance, an oscillator is constructed that uses the primary $LC$ tank as the frequency selective element [13]. A simplified schematic is presented in Fig. 7.

To understand the operation of the circuit, first assume that $\phi = 0$. Then the oscillation frequency is set to the point where the loop formed by the inverter, $R_{sense}$, and the comparator has 0 degrees of phase shift. Since the inverter and comparator each contribute 180°, their effects cancel. This forces the condition that $v_s$ is in phase with $i_t$, so the frequency must be the resonance of the tank, $f = 1/(2\pi\sqrt{LC})$.

If $\phi \neq 0$, then the effect will be to force an equal and opposite phase shift between the tank current and input

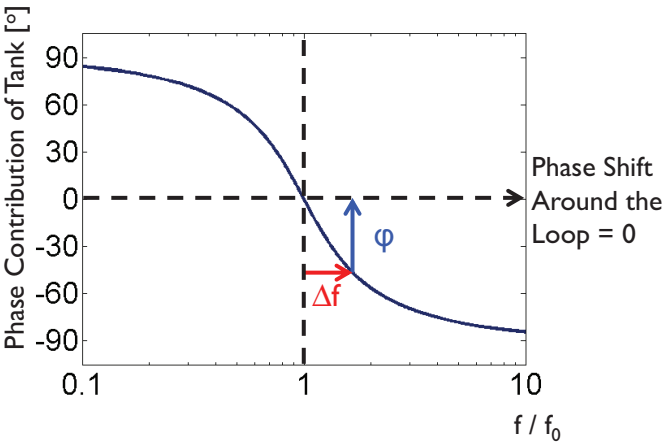


Fig. 8. Effect of introducing extra phase shift into the frequency control loop.

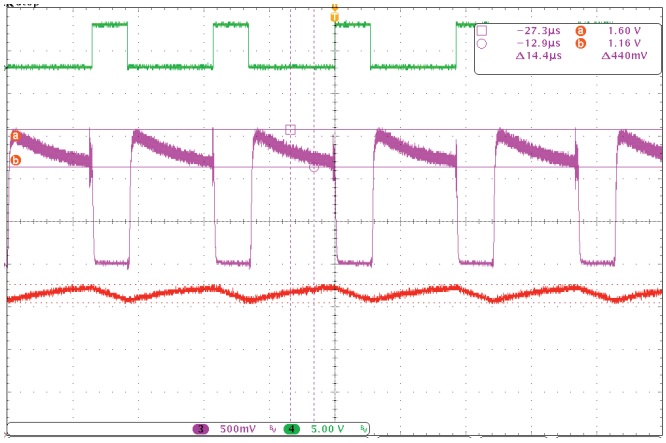


Fig. 9. Experimental results showing operation of multiperiod PWM loop. Top: SHUTDOWN signal. Middle: DC Component of supply current (40 mA/div). Bottom: DC output voltage (10 V/div). Timescale is 40 $\mu$s/div.

voltage, $\angle(i_t/v_s)$. This is illustrated in Fig. 8, which is a plot of $\angle(i_t/v_s)$ versus normalized frequency. For $\phi > 0$, the plot indicates that the oscillation frequency will shift up.

By setting $\phi$ equal and opposite to the phase shift calculated in the example design, the circuit is forced to run at the correct operating point. This also has the effect of regulating the output voltage because of the relationship derived in (4).

### C. Automatic Duty Cycle Control

In Section II, the ZVS condition was derived assuming a constant output power. In particular, (12) shows the specific relationship, which clearly does not hold for all $P_{out}$. This will cause the light load efficiency of the powertrain to suffer, as ZVS will not occur. Multi-period pulse-width modulation (MPWM) is used to solve this problem.

In MPWM, the transmitter is switched on and off, with a duty cycle scaled proportionately with the output power. The desired operation under a light load condition is presented in Fig. 9. The top trace is the SHUTDOWN signal; when high, the transmitter is off. The middle trace is the DC component of the current drawn from $V_S$ and the bottom trace is the DC output voltage.

The complementary duty cycle of SHUTDOWN is adjusted to the portion of full power that the load is drawing, in this case about 75%. When the transmitter is off, the load draws power from a hold-up capacitor, slightly discharging it. When turned back on, the supply current drawn will be the sum of the current required to recharge the hold-up capacitor and the load current. In this way, the average current drawn while the transmitter is running is always high enough to satisfy the ZVS condition, regardless of the load current.

As the hold-up capacitor is recharged, the supply current will decrease. This can be detected, and the transmitter can be shutdown until the beginning of the next MPWM cycle. This will result in the duty cycle being automatically adjusted to the load condition.

The the hold-up capacitor should be sized based on the allowable amount of ripple on the DC output voltage. The relationship between voltage ripple, power, frequency, and capacitance is given in [14].

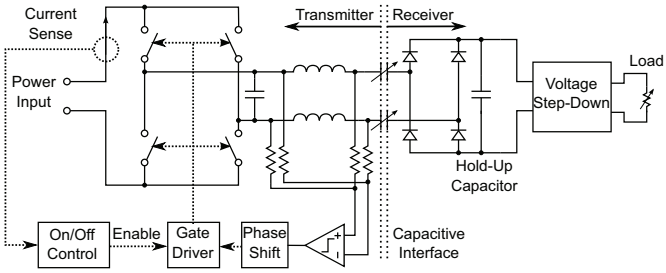


Fig. 10. Block diagram of CPT system including series resonant converter, automatic frequency control, and automatic duty cycle control.

### D. Experimental Results

Fig. 10 presents a block diagram of the designed system, composed of the pieces described above. Automatic frequency tuning was implemented by measuring the zero crossing of the inductor voltage rather than the tank current. Because the current is nearly sinusoidal, this simply results in 90° of phase lead, which is compensated for in the phase shift block. A relaxation oscillator embedded in the loop starts the circuit up then locks to the correct frequency.

MPWM is implemented with the on-off controller, which senses the average value of the supply current with a second-order low-pass filter. The filter is designed to attenuate the current component at twice the operating frequency while responding quickly to changes in the DC component. This current is compared with a reference. If it is less than the reference value, the gate drive circuit is disabled, and the powertrain is turned off. A 38.8 kHz clock forces the powertrain on for a minimum of 3.5 $\mu$s every cycle, which is enough time for the series resonant circuit to reach steady state. A 1 $\mu$F capacitor is sufficient to hold-up the output voltage under worst-case conditions. A limiter clamps the supply current to a safe value in case of a short circuit or cold-start condition.

The efficiency was measured for a range of output power

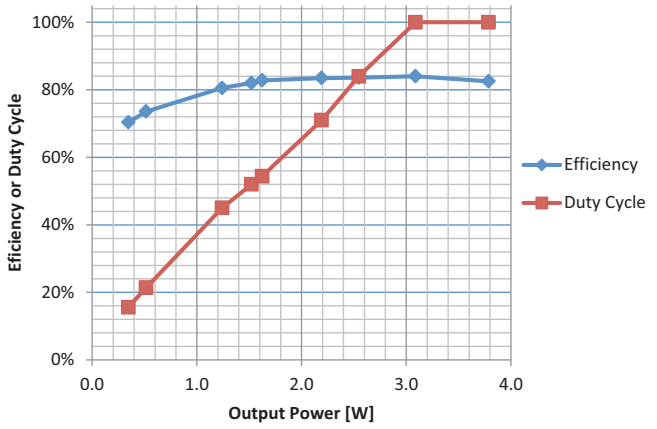


Fig. 11. Experimental data showing efficiency and duty cycle vs. output power for designed CPT system.

with $C = 156\,\mathrm{pF}$ (no added misalignment). The results are presented in Fig. 11; the loss of the final step-down is not included. The switching frequency was measured to be 4 MHz. To first order, the efficiency should remain constant across the range of output power, but because of the dynamics involved in turning the transmitter on and off, the efficiency slightly drops off at light loads. The peak efficiency is 84% at 3.2 W of output power. The duty cycle is also plotted in Fig. 11. The transmitter is always on until the output power drops below 3.2 W; this threshold is determined by the reference tank current. The duty cycle scales linearly with the output power below this point, as expected. Fig. 9, described above, was captured from this particular system running at 75% duty cycle.

## V. Conclusion

Small air gap capacitors enable high efficiency contactless power transfer. Their simplicity, small size, and low EMI makes them a very attractive solution for efficient charging of battery powered appliances such as smartphones. The key to high efficiency is series resonant operation using small and moderate Q ferrite core inductors, enabling soft-switching and high frequencies. Dynamically adjusting the operating frequency and duty cycle ensures high efficiency over a wide range of load conditions and accommodates large capacitance variations resulting, for example, from variations of alignment of the capacitor plates on the primary and secondary. This tuning is accomplished continuously in the background at the primary only, thus alleviating the need for a feedback loop from the load side back to the controller. Capacitive powering can be easily combined with high speed data transfer, enabling both charging and data synchronization over a single interface.

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