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Chip-Scale Coils for Millimeter-Sized Bio-Implants

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***Abstract*—Next generation implantable neural interfaces are targeting devices with mm-scale form factors that are freely floating and completely wireless. Scalability to more recording (or stimulation) channels will be achieved through distributing multiple devices, instead of the current approach that uses a single centralized implant wired to individual electrodes or arrays. In this way, challenges associated with tethers, micromotion, and reliability of wiring is mitigated. This concept is now being applied to both central and peripheral nervous system interfaces. One key requirement, however, is to maximize specific absorption rate (SAR) constrained achievable wireless power transfer efficiency (PTE) of these inductive links with mm-sized receivers. Chip-scale coil structures for microsystem integration that can provide efficient near-field coupling are investigated. We develop near-optimal geometries for three specific coil structures: in-CMOS, above-CMOS (planar coil post-fabricated on a substrate), and around-CMOS (helical wirewound coil around substrate). We develop analytical and simulation models that have been validated in air and biological tissues by fabrications and experimental measurements. Specifically, we prototype structures that are constrained to a 4 mm$\times$ 4 mm silicon substrate, i.e., the planar in-/above-CMOS coils have outer diameters $<$4 mm, whereas the around-CMOS coil has an inner diameter of 4 mm. The in-CMOS and above-CMOS coils have metal film thicknesses of 3-μm aluminium and 25-μm gold, respectively, whereas the around-CMOS coil is fabricated by winding a 25-μm gold bonding wire around the substrate. The measured quality factors (*Q*) of the mm-scale Rx coils are 10.5 @450.3 MHz (in-CMOS), 24.61 @85 MHz (above-CMOS), and 26.23 @283 MHz (around-CMOS). Also, PTE of 2-coil links based on three types of chip-scale coils is measured in air and tissue environment to demonstrate tissue loss for bio-implants. The SAR-constrained maximum PTE measured (together with resonant frequencies, in tissue) are 1.64% @355.8 MHz (in-CMOS), 2.09% @82.9 MHz (above-CMOS), and 3.05% @318.8 MHz (around-CMOS).**

***Index Terms*—Chip-scale coil, implantable neural microsystem, integrated coil, mm-sized coil, microfabricated coil, near-field coupling, wirewound coil, wireless power transmission.**

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I. Introduction

MILLIONS of people worldwide are affected by neurological and psychiatric disorders, in addition to damages to the nervous system due to stroke, spinal cord injury (SCI), or traumatic brain injury (TBI). Emerging technologies that provide the capability of direct neural interfacing offer the prospect of new therapies and treatments. Even at present, most human trials in Brain Machine Interfacing (BMIs) are utilizing percutaneous wired connections for powering and communication. Breaking through the skin (or tissue), however, poses a significant risk of infection [1]. A tethered approach additionally requires anchoring a rigid micro-electrode array (MEA) within soft, delicate tissue. Therefore, the associated micro-motion increases the risk of damage to the blood-brain barrier (BBB) that can lead to scar formation and failure of the device in the long run [2]. It is thus highly desirable to have devices that can avoid the tethering problem by utilizing Wireless Power Transfer (WPT) [3].

Over the past few years, there have been new efforts in developing wireless, free-floating microsystems that achieve scalability through a distributed approach, i.e. using multiple devices that are sub-mm or mm-scale. These devices are being developed for both the peripheral and central nervous systems, such as electroceuticals, and BMIs, respectively [4]–[9]. This concept is illustrated in Fig. 1, for a subdural BMI, utilizing near-field coupling for WPT.

Several methods have been proposed to power these sub-mm and mm-scale neural implants, including: ultrasonic [9], [10], midfield [11], and near-field powering [1], [12]–[16]. Ultrasound maintains efficient energy transmission for subcutaneous implants when they are perfectly aligned, but it is not suitable for powering distributed or intracranial implants due to its significant attenuation through the skull and extreme sensitivity on depth and orientation misalignments of the piezo-crystals. Midfield energy transmission results in significantly less allowable power delivered to the load (PDL) because of the higher specific absorption rate (SAR) in tissue at high frequencies instead, despite its ability in focusing the electromagnetic (EM) field on the location of the implant. Near-field WPT, on the other hand, has a few advantages as follow:

Firstly, the maximum allowable PDL is larger than that of the mid-field because of the lower SAR in the tissue at lower frequencies [17], [18]. Secondly, near-field WPT experiences negligible channel variations in tissue, as opposed to mid-field transmission, in which propagation delays dominate because of the inhomogeneous permeability of tissue at higher frequencies [19], [20]. Therefore, near-field WPT seems to be more suitable

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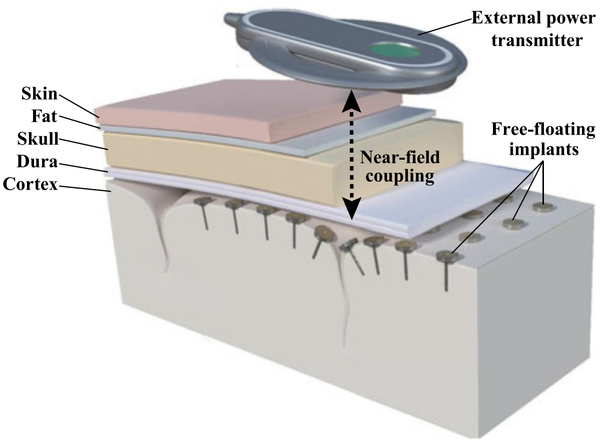

Fig. 1. Concept of a distributed implantable BMI with freely-floating neural probes that use mm-scale secondary coils for wireless powering.

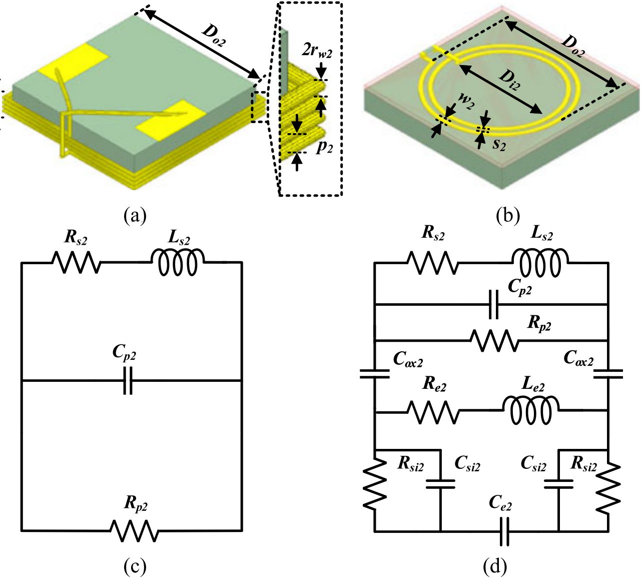

Fig. 2. 3D illustration for (a) around-CMOS (i.e. wirewound) coil; and (b) on-CMOS and above-CMOS (i.e. on substrate) coils, and equivalent circuit models for (c) around-CMOS coil and (d) on-CMOS and above-CMOS coils.

and reliable for powering the mm-scale implants through the lossy biological medium.

The power transfer efficiency (PTE) of inductive links to power mm-scale implants are often very low (a few percents) due to their relatively large coil separation, and arbitrary locations and orientations of implants [21]. There have been efforts to improve the SAR-constrained PTE for mm-scale devices and provide meaningful levels of PDL (0.1–1 mW) by optimizing the inductive link geometry [6], [13], [15]. Much of the work reported to date, including [22], focus on a single method wirewound coils (WWCs), and as such, do not explain the pros and cons of utilizing alternative technologies. For instance, there has already been much work in integrated coils for RFIC designs such as [12], [23], [24]. However, the quality factor (Q) of integrated coils remains limited ($<$10). This is because the CMOS technologies can only support metal layers that are relatively thin (1–4 μm), and suffers from losses due to eddy currents, particularly when the substrate resistivity is low [25]. Even using advanced techniques, such as multiple metal layers connected in parallel using vias [26], or patterned ground shields [27], result in modest gains. There have also been a number of CMOS-compatible MEMS technologies proposed to improve Q, such as developing suspended coils above the substrate [28], [29], or utilization of polymer enhanced through-silicon-vias [30].

We present different methods of developing mm-scale coils for integration with CMOS microelectronics for distributed implantable neural microsystems. We refer to them in the rest of this paper as *in-CMOS* (fully-integrated coils), *above-CMOS* (post-processed on top of CMOS substrate), and *around-CMOS* (wirewound around the CMOS chip). This study builds upon our earlier work [14], now extended to three types of coils by adding *above-CMOS* coils into our comparison. Also, *around-CMOS* coil has comparable dimensions (4 mm $\times$ 4 mm) to the *above-CMOS* and *in-CMOS* coils (previously this was 1 mm $\times$ 1 mm). Furthermore, we have derived analytical models, optimize design through computational methods, fabricated the coils, and compared their performance through measurements of the individual coils but also the 2-coil link in both air and tissue. Section II introduces analytical models for the different coil types. Section III describes the fabrication process for each coil type and optimization paradigm using simulation models to maximize the PTE. Section IV presents measurement results, while also exploring practical matters, such as electromagnetic properties, manufacturability, reliability and performance modification made by the presence of the tissue environment. Section V discusses the potential impact of integration with the rest of the implant, particularly the packaging on the coil performance, and the effects of surrounding tissue environment, followed by conclusions.

II. Analytical Coil Model

This section presents analytical models for three different types of coils; *in-CMOS*, *above-CMOS* and *around-CMOS*, for powering mm-sized implants. Key geometric parameters of the *around-CMOS* coil are illustrated in Fig. 2(a), where D_{o2} is the coil side length, r_{w2} is the wire radius, p_2 is the center-to-center pitch between adjacent turns, and l_2 is the solenoid length. Fig. 2(b) illustrates 3D model of a planar spiral coil, which is valid for both *in-CMOS* and *above-CMOS* types with key geometrical parameters: D_{o2} the outer diameter, D_{i2} the inner diameter, w_2 the trace width, and s_2 the spacing between adjacent traces. N_2 is the number of turns for all types of coils on the power receiving side. The equivalent circuit model with lumped RLC elements for *around-CMOS* and both *in-CMOS* and *above-CMOS* (substrate-based) coils are shown in Figs. 2(c) and 2(d) , respectively, where L_{s2} and R_{s2} are the series-connected inductance and parasitic resistance, and C_{p2} and R_{p2} are the parallel-connected parasitic capacitance and resistance, respectively. The parasitics elements associated with the substrate can be modeled by three components: R_{si2} the substrate resistance determined by majority carrier concentration, C_{si2} the substrate capacitance associated with high dielectric silicon media, and C_{ox2} the silicon oxide capacitance [21]. The eddy current through the silicon

substrate can be estimated using resistance R_{e2}, inductance L_{e2}, and capacitance C_{e2}. The geometry-dependent expressions that estimate the coils' self-resonance frequency (SRF) of mm-scale coils based on the lumped RLC elements in Figs. 2(c) and 2(d) are presented in the following subsections.

A. Around-CMOS (wirewound) Coil Model

Equivalent circuit model for around-CMOS coil is relatively simple because the silicon substrate does not significantly affect the electrical properties of this type of coil because of the sufficient spacing between the silicon substrate and coil conductors. The serial inductance L_{s2} of the *around-CMOS* coil can be found from [22],

$$L_{s2} = \mu_{eff}\pi r_{HF}^2 N_2^2 K_L K_P \tag{1}$$

$$K_L = 1/(l + 0.9004 D_{o2}/2), \tag{2}$$

$$K_P = 0.00875(p_2/r_{w2})^2 + 0.035 p_2/r_{w2} + 0.83, \tag{3}$$

where effective magnetic permeability U_{eff} is determined by the relative permeability of surrounding materials. K_L is a correction factor for the assumption of having a uniform magnetic field across the solenoid, and K_P models the effect of large pitch. r_{HF} is the effective wire radius considering the skin effect at operating frequency, and can be found from [22], equation (4) shown at the bottom of this page, where R_{s2} represents the sum of skin effect resistance, R_{sk}, and proximity effect resistance, R_{pr}, considering their orthogonality [31],

$$R_{s2} = R_{sk} + R_{pr} \tag{5}$$

where R_{sk} and R_{pr} can be expressed as:

$$R_{sk} = \frac{R_{dc} m}{2}\left(\frac{ber(m)bei'(m) - bei(m)ber'(m)}{(ber'(m))^2 + (bei'(m))^2}\right) \tag{6}$$

$$R_{pr} = \frac{-4\pi R_{dc} m}{\sigma}\left(\frac{ber_2(m)ber'(m) - bei_2(m)bei'(m)}{(ber(m))^2 + (bei(m))^2}\right)\left(\frac{H_n}{I_0}\right)^2, \tag{7}$$

$$m = \sqrt{\omega\mu_r\mu_0/\rho r} \tag{8}$$

where ρ is the metal resistivity, and H_n is the magnetic fields under the net current flowing through the solenoid coil I_0, μ_r is the relative permeability of the conductor. $ber(m)$ and $bei(m)$ are Kelvin functions [22].

C_{p2} and R_{p2} can be precisely modeled using equivalent lumped elements in series or parallel connection with coefficients for fitted curve polynomials estimated using COMSOL (Los Angeles, CA) simulation. Their equations and table containing the curve-fitting coefficients are described in [22].

B. In-CMOS and Above-CMOS (substrate-based) Coil Model

These coil types are based on planar spiral coils conductive substrate and thus have somewhat more complex analytical model, as shown in Fig. 2(d). The spiral inductance is estimated by using current sheet approximation [32].

$$L_{s2} = \frac{c_1\mu_{eff}{N_2}^2 d_{avg}}{2}\left(\ln\left(\frac{c_2}{\phi}\right) + c_3\phi + c_4\phi^2\right) \tag{9}$$

where

$$d_{avg} = \frac{d_{o2} + d_{i2}}{2}; \phi = \frac{d_{o2} - d_{i2}}{d_{o2} + d_{i2}} \tag{10}$$

Values for c_1 to c_4 can be found from [32], which only relate to the shapes of the planar spiral coils. N_2 is the number of turns and ϕ is the filling factor. Similar to *around-CMOS* coil, parasitic series resistance R_{s2} consists of R_{sk} and R_{pr}. R_{pr} is expressed in equation (7) and R_{sk} can be written as:

$$R_{sk} = \frac{R_{dc} t_2}{\delta(1 - e^{-t_2/\delta})} \tag{11}$$

$$R_{dc} = \frac{\rho l_2}{w_2 t_2}, \tag{12}$$

$$\delta = \sqrt{\frac{\rho}{\pi\mu_r\mu_0 f}}, \tag{13}$$

where t_2, w_2 and l_2 are the thickness, width and length of conductor tracks, respectively. Similar to the around-CMOS coil model, the parallel parasitic capacitance C_{p2} and the parallel parasitic resistance R_{p2} are caused by the dielectric loss of the coating materials and the biological tissues. In addition, this equivalent model contains the substrate capacitance C_{si2}, substrate resistance R_{si2}, and silicon oxide capacitance C_{ox2} [33].

$$C_{si2} = \frac{l_2 w_2 C_{Sub}}{2} \tag{14}$$

$$R_{si2} = \frac{2}{l_2 w_2 G_{Sub}}, \tag{15}$$

$$C_{ox2} = \frac{l_2 w_2 \varepsilon_{ox2}}{2 t_{ox2}}, \tag{16}$$

where C_{Sub} and G_{Sub} represent the unit capacitance and conductance of silicon substrate. t_{ox2} and ε_{ox2} are the thickness and permittivity of silicon dioxide. The current in the coil generates eddy currents on the silicon substrate that are not negligible and cause a parasitic inductance L_{e2} and resistance R_{e2} [34]–[36],

$$L_{e2} = 10^{-6} d_{o2}^{0.98} {w_2}^{4.39} {s_2}^{-0.99} {N_2}^{-1.84} L_{s2}^{0.68} \tag{17}$$

$$R_{e2} = 39{N_2}^{1.3}(w_2 + s_2)^{0.93} {l_2}^{-1.4}. \tag{18}$$

$$r_{HF} = \frac{0.5 D_{o2}(1 - (2r_{w2}/D_{o2})^2)(p_2/2r_{w2} - 1) + D_{o2} - 2r_{w2} + 2r_{w2}/N_2}{p_2/2r_{w2} + 1} \tag{4}$$

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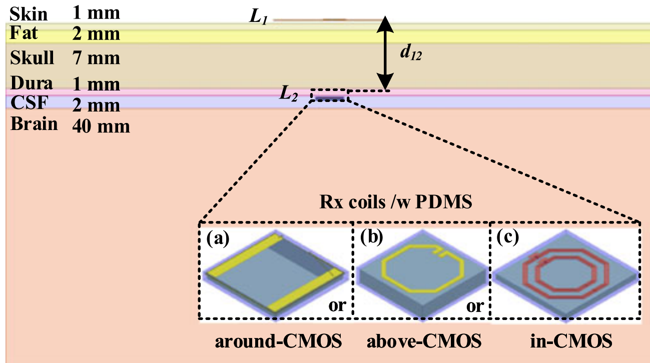

Fig. 3. Cross-section of the human head model and relative positions of the Tx and Rx coils. Inset: Rx coil models (a) *around-CMOS* (wirewound coil, WWC); (b) *above-CMOS* (microfabricated MEMS); (c) *in-CMOS* coils.

III. Coil Design and Fabrication

A. Simulation Setup

The electromagnetic (EM) simulation model of the inductive link is setup in HFSS (ANSYS, Canonsburg, PA) environment, which is a 3D full-wave EM field solver based on finite element analysis (FEA). Fig. 3 shows the cross-section of the EM simulation model of the mm-scale Rx coil, L_2, around a 10 cm$\times$ 10 cm $\times$ 5 cm human head model with a transmitter (Tx) coil, L_1, placed above it. The frequency-dependent dielectric properties of skin, subcutis (fat), skull (bone), cerebrospinal fluid (CSF), dura, and brain are fed into this EM simulation model based on [37]. The nominal distance between L_1 and L_2 is considered to be $d_{12} = 12$ mm, which is the nominal scalp-to-cortex distance [38]. The air-gap between L_1 and the skin is often a geometrical parameter to be optimized, but we have also fixed it to be 0.6 mm since d_{12} is fixed at 12 mm for fair PTE comparison among three types of coils. L_2 is placed in the CSF and covered with 100 μm of polydimethylsiloxane (PDMS). The center of L_2 is aligned with the center of L_1. These 2-coil inductive links aim to deliver 111 μW to 9 kΩ load resistance at 1 V_{rms} across the secondary LC tank. To allow for a fair comparison between these three coil types, the size of the silicon substrates is chosen to be 4 mm $\times$ 4 mm based on the estimates of the area needed for the implantable device integrated electronics.

Tx coils for three types of Rx Coils are individually optimized in air and tissue models to maximize the PTE of the 2-coil links in two different surrounding environment. Since Tx coils are located outside the body, this eases the size and material limitations, making it possible to use higher electrical conductivity copper (5.96 $\times$ 10^7 S/m) to design cm-scale Tx coils instead of gold (4.10 $\times$ 10^7 S/m) or aluminum (3.77 $\times$ 10^7 S/m) for Rx coils. Detailed specifications of the Tx coils are listed in Table I. The three different Rx coil structures are shown in the inset in Fig. 3: *around-CMOS* (with insulated bond-wire); *above-CMOS* (post fabricated); and *in-CMOS* coils. For the *around-CMOS* coil, an insulated Au bond wire with 25 μm diameter, $2r_w$, is wound around the substrate, with its terminals bonded to a pair of pads on the surface of silicon substrate. The *above-CMOS* coil is electroplated with a 25 μm thick Au layer on the silicon substrate. The *in-CMOS* coil is designed in HFSS and imported

TABLE I
Optimal Geometries and Electrical Properties of Rx Coils

Types	*Around-CMOS*		*Above-CMOS*		*in-CMOS*	
Medium	Air	Tissue	Air	Tissue	Air	Tissue
Material	Cu	Cu	Cu	Cu	Cu	Cu
L_1[nH]	29.9	38.5	42.9	20.2	46.5	24.56
R_1[Ω]	0.304	0.907	0.11	0.13	0.38	0.41
Q_1	370.8	80.2	269.55	58.58	321.2	124.2
D_{o1}[mm]	28	17.2	32	24	36	26
w_1[µm]	5000	600	6000	6000	6000	6000
t_1[µm]	70	70	35	35	35	35
p_1[µm]	N/A	N/A	N/A	N/A	N/A	N/A
N_1	1	1	1	1	1	1
Material	Au	Au	Au	Au	Al	Al
L_2[nH]	82.5	63.7	4.56	4.57	6.51	5.68
R_2[Ω]	10.05	4.97	0.15	0.09	1.47	1.39
Q_2	38.93	24.23	21.02	18.45	11.82	8.47
Q_{2L}	25.95	15.29	18.56	10.81	8.11	4.24
D_{o2}[mm]	4	4	4	4	4	4
w_2[µm]	25	25	250	250	175	175
t_2[µm]	25	25	25	25	4	4
p_2[µm]	30	30	N/A	N/A	N/A	N/A
N_2	2	2	1	1	1	1
d_{12}[mm]	12	12	12	12	12	12
k_{12}	0.013	0.0093	0.018	0.009	0.010	0.008
f_0[MHz]	600	300	110	60	426	330
PTE[%]	26.3	3.88	19	2.12	8.18	1.68

to the Virtuoso Layout Suite (Cadence Design Systems Inc., San Jose, CA). The fabrication process for the CMOS coil is AMS 0.35 μm 4M, 2P, 50 V technology (H35B4S1, ams AG, Austria). In this process, metal layers 1–3 are 640 nm, and top metal layer is 3 μm thick. The *in-CMOS* coil uses MET3 and MET4 layers connected in parallel (using VIA3) to increase the total metal trace thickness to 4 μm (considering the thickness of VIA3). Slots are added to metal traces to meet the design rules and relieve the surface tension of the metal layers.

B. Optimization

Fig. 4(a) shows the equivalent circuit model of 2-coil inductive link for powering mm-scale implants. For impedance matching at a target resonant frequency f_0, a tuning capacitor C_2 often connected with L_{s2} in parallel or series, depending on the value of the original load resistance $R_{L,O}$. In most cases for powering mm-scale implants, $R_{L,O}$ is in the order of kΩ, and a parallel C_2 is preferable since it results in a larger loaded Q factor, Q_{2L} [13], [22]. Fig. 4(b) shows the simplified equivalent circuit for all coils. The right side of Fig. 4(b) is a simplified equivalent circuit of both Figs. 2(c) and 2(d) when one side of the inductor is connected to ground and placed in series with C_2, where $R_L = wL_{s2}^2/(R_{L,O}||R_{p2})$. For a large load $R_L << |1/(jwC_{ox2}) + R_{si2}||1/(jwC_{si2})|$, the loss by the silicon substrate can be ignored. However, for most implantable applications, the loss through the silicon substrate cannot be negligible since $R_L \approx |1/(jwC_{ox2}) + R_{si2}||1/(jwC_{si2})|$. To minimize the substrate loss for the *above-CMOS* coil, several

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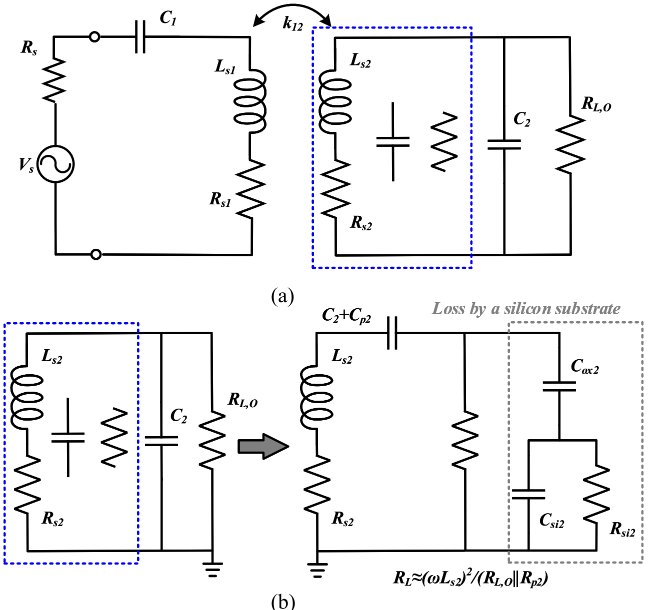

Fig. 4. Equivalent circuit models for: (a) 2-coil inductive link for powering mm-scale Rx coil; (b) mm-scale Rx coil with a silicon substrate.

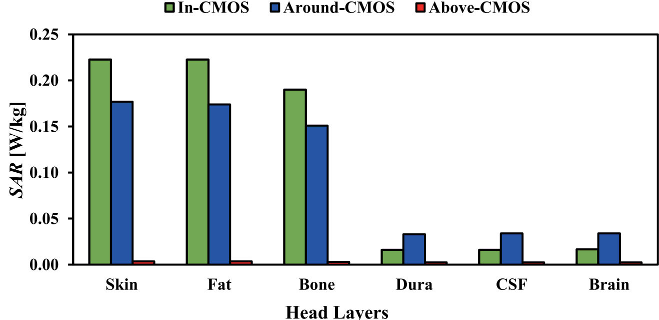

Fig. 5. Simulated SAR in head model at optimal frequencies for *in-CMOS*, *around-CMOS* and *above-CMOS* coils with fixed 10 mW Tx power.

techniques exist such as physically decoupling the coil from the lossy silicon substrate [28], [29] or replacing the silicon substrate with polymer [30]. As described in [13], [22], [39], because of the very small coupling, $\leq$0.01, between L_{s1} and L_{s2}, the geometric design and optimization of the Tx and Rx coils can be completed independently. Therefore, the PTE can be defined as [13],

$$PTE = k_{12}^2 Q_1 Q_{2L} \eta_{Rx} = Tx_{FoM} Rx_{PRS} \tag{19}$$

where Tx figure of merit (FoM), Tx_{FoM}, represents the coupling strength between Tx and Rx coils. Rx power reception susceptibility, Rx_{PRS}, indicates how much power can be received and passed to R_L [13]. k_{12} is the Tx-Rx coils' coupling coefficient. Q_1 and Q_{2L} are the Q factors of the Tx and loaded Rx coils. η_{Rx} is the ratio of the power delivered to R_L to the power dissipated in the secondary coil due to its parasitic resistance, R_{s2}.

1) Optimizing Rx: After applying the common design constraints such as $D_{o2} = 4$ mm, each coil was designed by following the coil optimization procedure in [13], [15], [40] in a way to maximize Rx_{PRS}, which is a multiplication between the loaded Q factor, $Q_{2L} = wL_{s2}/(R_{s2} + R_L)$, and the Rx internal efficiency, $\eta_{RX} = R_L/(R_2 + R_L)$). For the *around-CMOS* design, p_2 is fixed because this design parameter is not controllable during the semi-manual coil fabrication. Considering the diameter of the commercially available insulated bonding-wire, $2r_w$ is chosen to be 25 μm. N_2 was swept in the HFSS model and MATLAB (MathWorks, Natick, MA) using the analytical model presented in Section II. For the design of *in-CMOS* coil, the thickness and material of metal layers are defined by the CMOS process, consequently, its Q_2 is mainly limited by series resistance R_{S2} [28]. The geometric optimization for the *in-CMOS* coil thus focuses on the number of turns N_2 and width-to-spacing ratio w_2/p_2 [41]. Gold (Au) is selected for *above-CMOS* coil for its high conductivity and biocompatibility. In addition, the thickness of the metal traces is not limited by the CMOS process, and can be optimized in HFSS and fabricated up to a certain limit by electrochemical deposition to reduce R_{S2}.

The optimal geometry of the Rx coil in the tissue medium often tends to have fewer turns and a smaller trace width than the one in air. This means that the coil has a smaller contact surface with the lossy tissue medium. The geometric dimensions of three Rx coils have thus been individually optimized in the human head model for IMDs. They have then been simulated in the air environment to reveal alterations of EM properties with the presence of biological tissues. The geometries and electrical properties of these coils after optimizations are shown in Table I.

2) Maximizing PTE: Since the PTE is a multiplication of Tx_{FoM} and Rx_{PRS}, the Tx geometry to maximize the PTE is explored in this subsection. PTE is largely dependent upon k_{12} in Tx_{FoM} (PTE $\propto k_{12}^2$). k_{12} is a spatial function of the geometrical dimensions of L_{s1}, L_{s2}, and d_{12} as [42],

$$k_{12} = \frac{1}{\left[1 + 2^{-4/3}\left(\frac{d_{12}}{\sqrt{D_{o1}D_{o2}}}\right)^2\right]^{3/2}} \tag{20}$$

where D_{o1} is the outer diameter of the Tx coil. (20) implies that k_{12} is dependent mostly on D_{o1} considering that D_{o2} is a Rx design constraint and d_{12} is fixed at 12 mm for this study. Therefore, the optimal D_{o2} was found first to maximize k_{12} and rest of Tx parameters were found to achieve the maximum Tx_{FoM}. The geometrical and electrical parameters of the 2-coil inductive link for three different Rx coils are summarized in Table I.

The operating frequency of each inductive link is individually optimized by adopting the methodology in [13], [15], [40]. According to optimized simulation results in Table I, *around-CMOS*, *above-CMOS* and *in-CMOS* coils in biological tissue environments operate at 300 MHz, 330 MH and 60 MHz, respectively. To ensure the human exposure to electromagnetic radiation at these frequencies within the safe levels, the SAR of these 2-coil links have been simulated with the fixed 10 mW transmitting energy and reported in Fig. 5. The operating frequency of the *above-CMOS* coil is relatively low compared to

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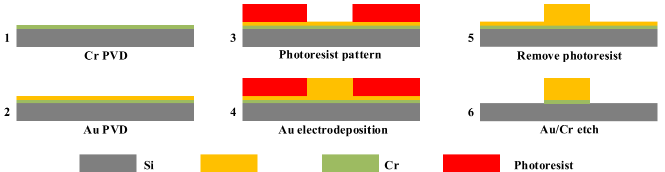

Fig. 6. Process steps of the *above-CMOS* (micro-fabricated) coil.

the others, so its SAR dramatically drops to 3.57E-3 W/Kg. The rest of the two Rx coils operate at higher frequencies and their SARs are below 0.25 W/Kg, which is far below the IEEE safety standard of 1.6 W/Kg [18].

C. Fabrication

Implementation of the *above-CMOS* (micro-fabricated) coil requires mainly photolithography and electroplating processes. Fabrication procedure of the *on-CMOS* coil is shown in Fig. 6. A 50 nm chromium (Cr) adhesive layer and 100 nm Au seed layer are deposited on a 4-inch silicon wafer using electron-beam physical vapor deposition (PVD). Subsequently, the AZ4562 photoresist (Microchemicals GmbH, Germany) is spin coated twice on the wafer at 1400 rpm for 40 s to reach 25 μm thickness. The profiles of coils are exposed and developed on photoresist layer by Dilase 250 photolithography system (Kloe, France). Then, 25.1 μm Au layer is added by electrochemical deposition. Following 183 min electroplating, the remaining photoresist and global thin Au/Cr layers are removed.

The *around-CMOS* coil is fabricated by winding a 25 μm insulated bondwire (Microbonds, Canada) around the 4 mm $\times$ 4 mm passive silicon die with a manual wire-bonder (Westbond 7476D, Anaheim, CA) and a stepper motor. The silicon die was fixed in the center of a QFN package. One terminal of the bonding-wire is ultrasonically bonded on the QFN package, which is placed on top of the stepper motor. The silicon die is then slowly rotated by the stepper motor, and position of the wedge is carefully adjusted in a way that the bonding wire is wound around the silicon die. Once the motor is revolved up to the target number of turns, the other end of bonding-wire is ultrasonically bonded on the QFN package. Afterwards, instant glue is applied to the four corners of the die to fix the coil in place. In an actual implant, two ends of bonding-wire will be attached directly on the active CMOS chip. In this case, however, they are lifted along with the passive silicon die and attached to designated pads on a PCB for measurements. Details of the fabrication procedure can be found in [6].

As described in Section II, the *in-CMOS* coil is fabricated in AMS 0.35 μm CMOS technology featuring a 3 μm thick top metal layer, and the top two metal layers are connected using VIA3 to create a 4 μm thick metal trace. The 10 μm slots are added to the metal trace to extend the effective width of the metal trace to 175 μm. Two terminals of the coils are connected to the 100 μm $\times$ 100 μm pads, which are arranged for ground-signal-ground-signal-ground (GSGSG) of RF probes.

The abovementioned coils are shown in Fig. 7. The inner octagonal shape coil in Fig. 7(c) is not relevant to this Rx coil comparison study.

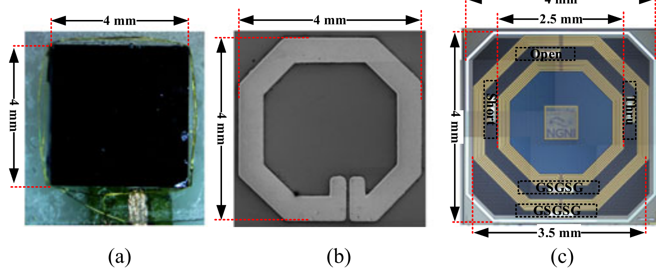

Fig. 7. Fabricated (a) *around-CMOS*; (b) *above-CMOS*; and (c) *in-CMOS* coils.

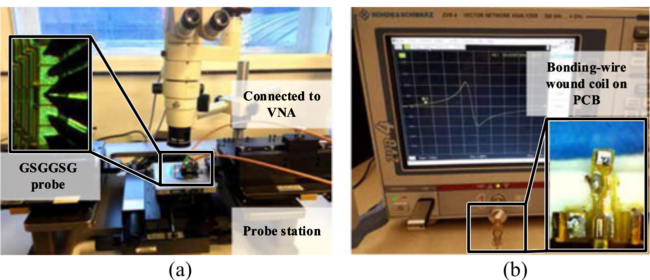

Fig. 8. In air measurement setups for: (a) the planar (*in-CMOS* and *above-CMOS*) coils; and (b) the wirewould (*around-CMOS*) coil.

IV. Results

A. Measurement Setup

1) In Air Measurement Setup: The planar (*in-CMOS* and *above-CMOS*) coils are measured using E8361A network analyzer (Agilent, CA), Model 40A probe (Picoprobe, FL, USA), ACP350 probe (Cascade Microtech, Oregon, USA) and probe station (Cascade Summit 9101, OR, USA). The measurement setup is shown in Fig. 8(a). To calibrate the network analyzer, the fabricated patterns for short-open-load (SOL) are utilized to eliminate parasitics from the cable and probes.

The *around-CMOS* coil is measured using a ZVB4 vector network analyzer (Rohde & Schwarz, Germany) in Fig. 8(b) measurement setup. The coil terminals are bonded to two pads on a T-shaped PCB that is connected to an SMA connector. To reduce the parasitic effects, measurements were calibrated using the de-embedding method. It involves subtracting the Y-parameters of the open-circuited PCB to remove the parasitic capacitance and resistance in parallel and subtracting the Z-parameters of the short-circuited PCB to remove the series parasitic inductance and resistance [13].

2) Ex vivo measurement setup: Fig. 9 shows the experimental setup for *ex vivo* measurements. The fresh 11 mm lamb ribs are inserted between the Tx and Rx coils. The Rx coils connect to a 2 cm $\times$ 5 cm PCB with an SMA connector via bonding wires, and the Tx coils are fabricated by utilizing 1 oz copper PCB and 2 oz copper foil. Both coils are tuned to the optimal operating frequency by using tuning capacitors, according to the simulation results in Table I. In addition, the impedance matching networks guarantee that the energy can be injected into the 2-coil inductive links from the VNA standard 50 Ω ports.

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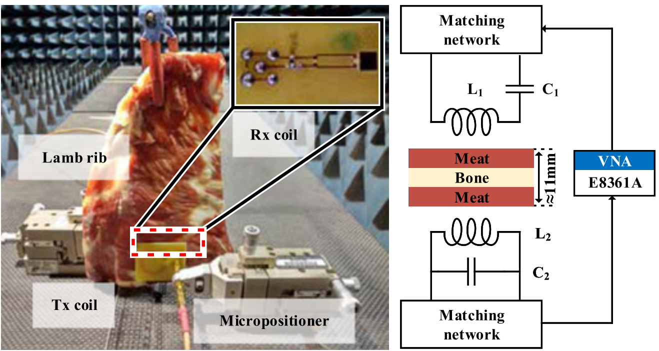

Fig. 9. *Ex vivo* measurement setups: (a) 2-coil links measured with lamb rib and (b) schematic of measurement setups.

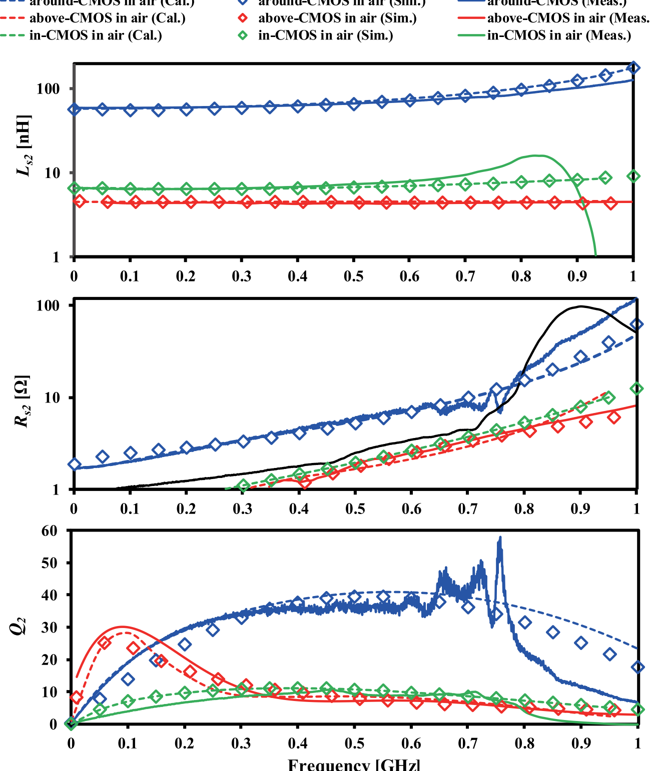

Fig. 10. In air measured *around-CMOS* wirewound (blue), *above-CMOS* micro-fabricated (red), and *in-CMOS* integrated (green) coils compared with simulated and calculated results showing: (a) inductance; (b) resistance; (c) Q factor.

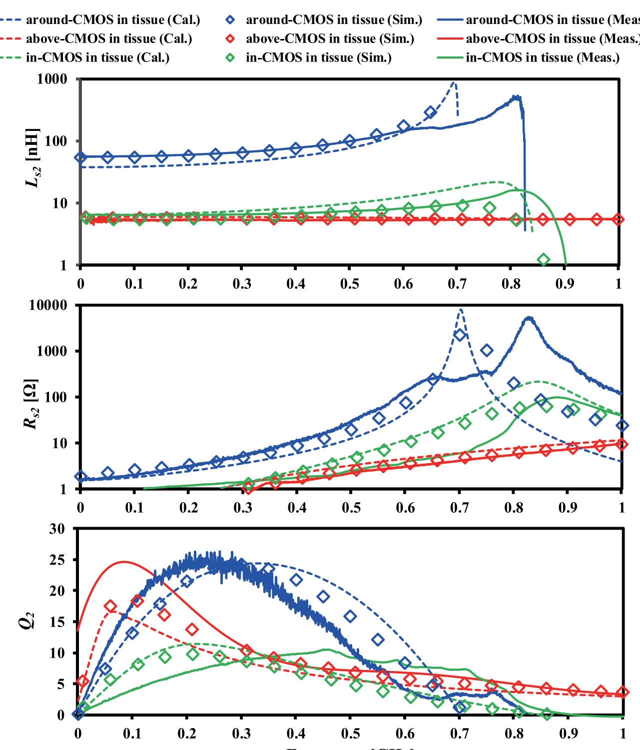

Fig. 11. *Ex vivo* measured *around-CMOS* wirewound (blue), *above-CMOS* micro-fabricated (red), and *in-CMOS* integrated (green) coils compared with simulated and calculated results showing: (a) inductance; (b) resistance; (c) Q factor.

B. mm-scale Rx coils

Fabricated *around-CMOS*, *above-CMOS*, and *in-CMOS* coils are individually measured in air and tissue sample from lamb rib (containing relevant thicknesses of tissue, fat and bone), as shown in Figs. 8 and 9, respectively. Calculated and simulated values are compared with measured results to validate analytical and simulation models. Figs. 10(a), 10(b), and 10(c) show the L_{s2}, R_{s2}, and Q_2 of the fabricated *around-CMOS*, *above-CMOS*, and *in-CMOS* coils, measured in air. The inductance of the coil remains constant when operating frequency is much lower than SRF. Under this condition, the measured inductance values are consistent with the calculated and simulated results. Meanwhile, their resistances significantly increase, due to skin and proximity effects, resulting in inaccurately calculated resistances at high frequencies. This is one of the reasons that cause slight deviation in Q factors between the measured, calculated, and simulated results in Fig. 10.

The alterations of Rx coils' electromagnetic properties with presence of tissue are shown in Figs. 11(a), 11(b), and 11(c). Compared with measured results in air and tissue, surrounding tissue environment mainly causes the significant increment of the resistance R_{s2} and reduces their SRF, resulting in lowering their maximum Q factors. In addition, the obvious deviations between measured values and calculated/simulated results in Fig. 11 are caused by the unpredictable parasitic components R_{p2}, C_{p2} due to the heterogeneous tissues medium, as shown in Fig. 2(d). The detailed EM characteristics of the three coils are described below.

1) Around-CMOS coil: The HFSS simulation results in air match well with calculated results from the analytical coil models in Section II across the entire frequency range up to 1 GHz. The measured L_{s2} and R_{s2} start deviating from their calculation and simulation by more than 3% and 15%, respectively, at 650 MHz. This deviation between the measured and simulated/calculated response comes from the approximation made in de-embedding when subtracting the Z-parameters of the short-circuit PCB from the Z-parameters of the device-under-test (DUT). The parasitic resistance and capacitance of the interconnect (PCB+SMA) in parallel with the network analyzer port

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are often ignored at low frequency. At high frequency, however, the parallel parasitic capacitance and resistance cannot be ignored, and cause some measurement inaccuracy over 650 MHz. Therefore, the measured resistance of the interconnects is below the actual value. This leads to R_{s2} being higher than its simulated or calculated value at high frequency. On the other hand, the measured inductance of the interconnect is above the actual value, and makes L_{s2} being lower than its simulated or calculated value at high frequency. The maximum Q_2 measured in air is 37.5 at 555 MHz where $L_{s2} = 69.5$ nH and $R_{s2} = 6.47$ Ω, compared to 26.23 at 283 MHz in the vitro measurements.

2) Above-CMOS coil: According to Figs. 10(a) and 11(a), L_{s2} of this *above-CMOS* coil in the air and in the tissue are 4.37 nH and 5.43 nH. Both measured inductance of the one-turn coil is consistent with simulated and calculated results. In Fig 10(c), there are slight deviations in the Q factors' curve between measured and simulated results when frequency is ≤300 MHz. It This is because the parasitic series resistance R_{s2} of the metal trace is extremely small (∼1.93 mΩ/□) at low frequencies (<300 MHz). It is difficult to accurately measure R_{s2} through de-embedding techniques due to the resistance of short circuit structure, resulting in slightly higher measured Q factors than the simulated and calculated results. The trend of measured Q factor, however, is consistent with the simulation results. The highest Q factor is 30.09 at 90.4 MHz, where L_{s2} and R_{s2} are 4.37 nH and 0.08 Ω. When this coil is placed in the tissue medium, the deviations between the measured Q_2, R_{S2} and the calculated and simulated values become significant, as shown in Fig. 11(a) and 11(b). This is due to the parallel parasitic capacitance C_{p2} and resistance R_{p2} formed between the above-CMOS coil and the tissue medium. These parasitic components cause not only the reduction of a Q factor from 30.09 @90.4 MHz to 24.61 @85.0 MHz, but also the deviations between calculated and measured results. The dielectric properties of the biological tissue are difficult to accurately estimated, so inaccurate parasitic parameters C_{p2} and R_{p2} in the analytical models cause the deviations between calculations and measurements. The deviations between simulation and measurement are caused by the homogeneous biological tissues in the simulation environment, but the real biological tissues have heterogeneous structures. In addition, *ex vivo* measurements are performed in lamb ribs, whereas calculations/simulations are setup in human brain model. The differences between the two environments also cause deviations between the measurements and the calculated/simulated results.

3) In-CMOS coil: The HFSS simulation results are consistent with the calculated results. The measurement results, however, deviate from the calculated and simulated results for frequencies ≥500 MHz. This is mainly caused by the discrepancy in SRF, which measured in the air and simulated values are 940 MHz and 1.35 GHz, respectively. The simulated SRF is higher than the measured result because the HFSS model is simplified due to limited computing resources. For instance, parasitic capacitances caused by dense vias and metal fill have not been considered. According to the measurement results shown in Fig. 10, the highest Q factor of the *in-CMOS* coil is 10.5 at 449 MHz, where $L_{s2} = 7.05$ nH and $R_{s2} = 1.89$ Ω. Similar to above-CMOS coils, the L_{s2}, and R_{s2} in the tissue medium slightly increase to 7.11 nH and 1.92 Ω, respectively, with the largest Q factor remaining at 10.50 @ 450.3 MHz.

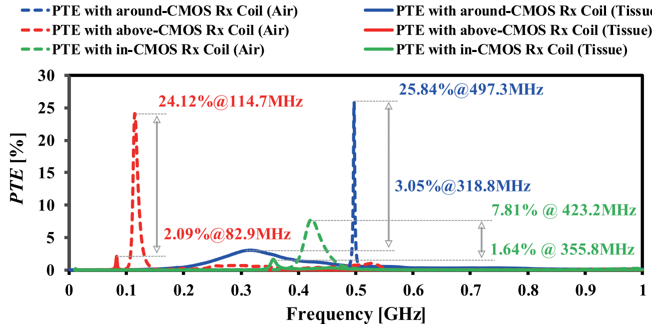

Fig. 12. Measured PTE of 2-coil inductive links to deliver power to the 4 mm × 4 mm *around-CMOS*, *above-CMOS*, and *in-CMOS* Rx coils.

C. Two-Coil Inductive Link

Fig. 12 shows the measured PTE of three types of 2-coil inductive links at the optimized operating frequencies in the air to power up three different mm-scale Rx coils. Since these Rx coils have their maximum Q factors at different operating frequencies, the geometries of Tx coils are individually optimized to maximize the PTE following the optimization methodology in [13]. Single-turn Tx coils were fabricated either from 70 μm thickness copper foil or RO4000 hydrocarbon ceramic laminates PCB with 1 oz copper (Rogers Communications Inc., Canada) using a PCB milling machine. The geometries of three fabricated 2-coil inductive links are summarized in Table I. All of the Tx coils and Rx coils are tuned at the desired operating frequencies with capacitors connected in series and parallel, respectively. The S-parameters of each fabricated 2-coil inductive links were measured with the network analyzer (Rohde & Schwarz ZVB4). The source impedance of the network analyzer, R_s, shown in Fig. 4(a) often kills the Q factor of the Tx coil, and results in lower measured PTE. To lower R_s from 50 Ω to 0.657 Ω, we connected a 63 pF capacitor in parallel with the port1 of the network analyzer, and compensated the loss of this matching network from the measured S-parameters of two-coil inductive link. To remove the coupling between the feed-line and Tx coil, we utilized de-embedding technique, subtracting the S-parameters between the Tx coil and the feed-line from the measured S-parameters of the two-coil inductive link, described in [13]. The PTE of each coil link were calculated based on the equation [15],

$$PTE = 100\% \times |S_{21}|^2 \times R_L/50 \tag{21}$$

where S_{21} is measured forward voltage after de-embedding of the feed-line at the Rx side and compensation of the matching network at the Tx side. The coil separation, d_{12}, was fixed at 12 mm for fair comparison among three fabricated links.

The maximum achievable PTE of the inductive link for the *around-CMOS*, *above-CMOS*, and *in-CMOS* coils are 25.84%, 24.12%, and 7.81% at resonating frequencies, 497.3, 114.7, and 423.2 MHz, respectively. The SAR-constrained maximum PTE

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TABLE II
COMPARISON BETWEEN *around-CMOS*, *above-CMOS*, AND *in-CMOS* COILS

Parameters	[Unit]	[43]	[6]	This work	[28]	[30]	This work	[12]	This work
Type	-	*around-CMOS*	*around-CMOS*	*around-CMOS*	*above-CMOS*	*above-CMOS*	*above-CMOS*	*in-CMOS*	*in-CMOS*
Diameter (D_{o2})	[mm]	1	1	4	0.3	1.53×1.03	4	2	4
Trace width (w_2)	[μm]	25	25	25	20	55-65	250	140	175
Trace spacing (s_2)	[μm]	25	-	-	30	100	-	40	-
Trace thickness (t_2)	[μm]	25	25	25	10	8-12	25	-	4
Number of turns (N_2)	-	5	7	2	4	1.5	1	4	1
Inductance (L_{s2})	[nH]	40	94	60.7	3.19	1.14	5.43	70	7.11
Resistance (R_{s2})	[Ω]	2.2	-	3.12	3.32	-	0.12	-	1.92
Q factor (Q_2)	-	50	22	26.23	25.7	55	24.61	11.05	10.5
Frequency@Q_{max}	[MHz]	400	130	283	13700	6750	85	100	450.3
SRF	[GHz]	-	-	-	14	21	1.9	0.22	0.9
PTE	[%]	-	9.13 (3-coil)	3.05	-	-	2.09	-	1.64
Frequency@PTE_{max}	[MHz]	-	275	318.8	-	-	82.9	-	355.8
Medium	-	Air	Tissue	Tissue	Air	Air	Tissue	Air	Tissue

in biological tissue environments for these coils are 3.05%, 2.09%, and 1.64% at operating frequencies, 318.8, 82.9, and 355.8 MHz.

V. DISCUSSION

Geometric parameters and electrical properties of the three fabricated coils are summarized in Table II and compared to the state-of-the-art. Since the metal traces of the *in-CMOS* and *above-CMOS* coils are in close proximity of the silicon substrate, their Q factors are degraded by the loss in the silicon substrate due to eddy current effects. Their Q factor decreases from wL_{s2}/R_{s2} roughly to $wL_{s2}/(R_{s2} + R_{si2}/(w^2C_{si}^2))$, as shown in the right part of Fig. 4(b). The optimal geometries for both *in-CMOS* and *above-CMOS* coils ends up with shorter l_2 and wider w_2, and result in much smaller L_{s2} and R_{s2} compared to those for the *around-CMOS* coil. The *around-CMOS* coil achieves the highest Q factor among three coils. The Q factor of the *above-CMOS* coil, however, has room for improvement by increasing the spacing between the coil further and lossy silicon substrate [28], [29] or replacing the silicon substrate with the polymer [30], at the expense of increased complexity. The standard CMOS process limits further improvement in the Q factor of *in-CMOS* coil. The predefined thickness of the metal layer in commercially available CMOS technologies limits its Q factor to ∼10 [12]. The patterned ground shielding in [27] may slightly improve the Q factor, but it is not comparable to those of the *above-CMOS* and *around-CMOS* coils. The main advantages of *in-CMOS* coils are well-controlled process, cost-effectiveness, smaller volume, and ease of mass production.

The *around-CMOS* coil has more variability in its electrical properties, particularly in the current manual fabrication process. A semi-automated fabrication can reduce these variations to less than 6% [44]. Uniformly wounded bonding wire around a predefined cylinder by a high-end fully automated wire-bonder can effectively reduce these process variations and increase Q factors of bonding wire coils with more delicate control on the coil geometry [43].

Design considerations, electrical properties, and fabrication methods of three mm-scale Rx coils with optimal geometries can guide implantable medical device (IMD) designers. For example, next generation free-floating mm-scale neural probes are likely to have embedded power coils [44]–[46]. As shown in Fig. 13(a), the free-floating wireless implantable neural recording system (FF-WINeR) proposed in [44] combines a 6-turn bonding-wire wound coil with a neural recording application specific integrated circuit (ASIC) and achieves high Q factor for the Rx power coil. As shown in Fig. 13(b), the empowering next generation implantable neural interfaces (ENGINI) [7], [45] stacks up a MEMS coil on its neural recording ASIC. Using a separately fabricated single-turn MEMS coil, ENGINI can save the silicon area for active circuits and achieve fairly high Q factor for the Rx coil as well. The encapsulated neural interfacing acquisition chip (ENIAC) [46], shown in Fig. 13(c), uses an integrated CMOS coil with active circuits. Integration with mm-scale coils, however, involves some challenges. Metal routing on the ASIC can cause considerable loss in addition to the loss from silicon substrates due to creating extra eddy current loops [41]. The layout of metal routing needs to be carefully designed without creating any loop. The biocompatible and hermetic encapsulation of the probes also reduces the Q factors and the PTE of the inductive links especially at high

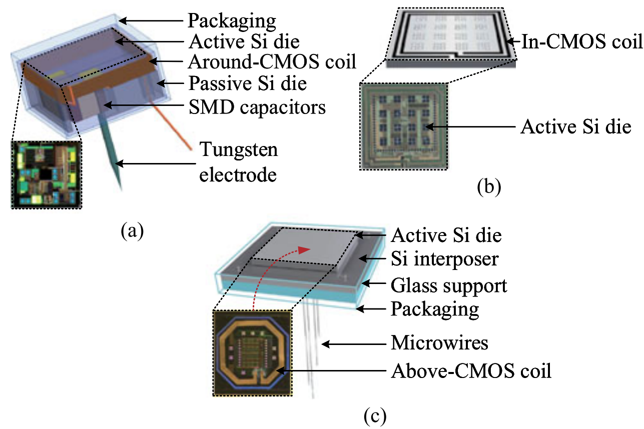

Fig. 13. Different concepts for probe integration with mm-scale coils: (a) Free-floating wireless implantable neural recording system (FF-WINeR) with an around-CMOS coil [44]; (b) Empowering next generation implantable neural interface (ENGINI) with an above-CMOS coil [45]; (c) Encapsulated neural interfacing acquisition chip (ENIAC) with an in-CMOS coil [46].

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frequency. Because higher permittivity and loss tangent of the surrounding package and tissue create additional paths for signal loss at high frequency [44]. Furthermore, the higher parasitic capacitance from the surrounding package and tissue lowers the resonant frequency of the mm-scale coils. Therefore, the tuning capacitance should be carefully determined considering these parasitic effects during the design stage, especially when designers integrate on-chip tuning capacitors in the ASIC. The detuned resonant frequency from the desired frequency can be compensated by an auto-resonance tuning (ART) circuit [47].

VI. Conclusion

This work has investigated three different mm-scale receiver (Rx) coil types: *in-CMOS*, *above-CMOS*, and *around-CMOS*. To ensure a fair comparison, the different coil geometries have been optimized following the same design procedure either on, or around an identical sized silicon substrate (4 mm $\times$ 4 mm). To accurately characterize their electrical properties in comparison with calculation and simulation, we have developed analytical and simulation models in MATLAB and HFSS, respectively. These models have been validated in the tissue environment with supporting experimental measurements. The analytical model, fabrication procedure, and characterization for each type of coil in the same dimension with optimized geometries guide researchers in mm-scale coil selection and design. Furthermore, the SAR-constrained maximum PTE in biological tissue using each type of Rx coil has been explored and compared with maximum achievable PTE in air to demonstrate the effect of tissue on WPT.

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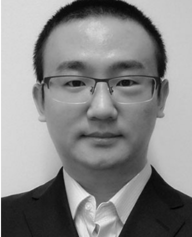

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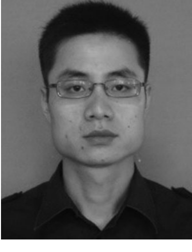

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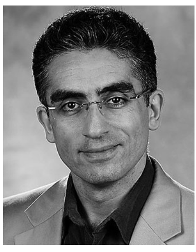

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