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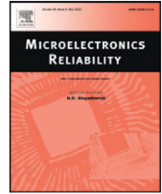

Influence of gate oxides with high thermal conductivity on the failure distribution of InGaAs-based MOS stacks

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ABSTRACT

In this work, the breakdown transients of metal-oxide-semiconductors (MOS) stacks with InGaAs channels and different oxide layers (Al_2O_3, HfO_2 and Si_3N_4) have been studied in terms of the time-to-breakdown and the duration of the progressive breakdown regime. It is observed that dielectric layers with higher thermal conductivity show larger transient time during the progressive breakdown regime, and this provides a significant lifetime extension across the entire failure distribution. This is attributed to a lower temperature of the percolation path which reduces local electro-migration. Moreover, the overall results show that the progressive breakdown regime is uncorrelated with the initial degradation rate, and that the bending of failure distribution at low percentiles is exclusively attributed to the progressive increase of the gate current during the breakdown event.
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1. Introduction

The introduction of InGaAs as a channel material for complementary metal-oxide-semiconductor technology (CMOS) presents major challenges in terms of the characterization of the various defects that affect the performance and reliability [1]. It has been reported in ultra thin gate insulators that the breakdown event (BD) is characterized by a progressive growth of the current and not an abrupt change in the conduction mechanism [2–4]. This effect occurs with Poly-Si or metal gate electrodes, with SiO_2, SiO_xN_y or high-k dielectrics as gate oxides, and with Si or InGaAs substrates, and must be taken into consideration for an accurate projection of the reliability of such technologies.

In ultra-thin gate oxide, after the BD event, there is a gradual process with the gate current increasing in a continuous progression from insulating to eventual shorting. Taking into account this progressive behavior of the BD event, the chip failure is redefined as a gate leakage level rather than the first jump in gate current, affecting the failure distribution of the gate oxide [2]. Contrary to thicker oxides, this updated cumulative distribution of the oxide failure has been found to be non-Weibull with two regions: a shallower slope at long times and a steeper slope at short times [5,6].

At the present some aspects of such cumulative failure distribution remains controversial. Some authors suggest that the bending of failure distribution at short times is exclusively attributed to differences in the defect generation rates between the high-k layers and its interfacial layer with larger Weibull slope at low percentiles [7,8].Although, a recent paper [9] shows for Hf-based high-k/Si stacks that the progressive BD (PBD) play a major role, it is not clear if it is a general effect observed in different dielectrics layers. In particular, there is no experimental data reported in the literature regarding the high-k/InGaAs stacks, which seems to be one of the frontrunner candidates for future CMOS nodes.

Another controversial topic is the occurrence of multiple competing BD events during the progressive BD regime. Some authors reported for SiON/Si stacks, that the apparent distribution of the PBD time was no longer area independent due to the multiple-BD effect [10], making difficult the identification of the PBD regime, and affecting the calculation of the failure distribution [11].

To clarify those controversial topics it is therefore interesting to investigate the behavior of the failure distributions in terms of the duration of the progressive BD. Here, we report experimental data of BD transient of MOS stacks with different dielectric layers (HfO_2, Si_3N_4 and Al_2O_3) but similar metal gate and substrate (InGaAs). The use of dielectric layers with different BD transient characteristics allow a deep analysis of the influence of the progressive BD regime in the failure distribution of the gate oxide, particularly at low percentiles. Regarding the occurrence of multiple-BD effects, a deep analysis of the physical effect during the PBD regime is performed to clarify the main conditions of the occurrence of multiple-BD paths.

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2. Experimental

In this work different MOS structures were fabricated with different dielectric layers: Al_2O_3, Si_3N_4 and HfO_2. In all cases an n-type InGaAs substrate (epitaxially grown on InP wafers) and gate metallization of Ti(1 nm)/Au(200 nm) were used. The area of the devices was 1.1×10^{-4} cm^2.

For the MOS structure with Al_2O_3 dielectric layer, a pre-dielectric deposition treatment (PDT) was performed by a NH_4OH solution, and then a 9 nm-Al_2O_3 layer was prepared by atomic layer deposition (ALD) using trimethylaluminium (TMA) and H_2O precursors at 300 °C. For the MOS structures with Si_3N_4, the dielectric was deposited by plasma enhanced chemical vapor deposition (PECVD) with NH_3 pre-deposition treatments. For the MOS structures with HfO_2, a pre-dielectric deposition treatment (PDT) was performed and then a 10 nm-HfO_2 layer was prepared by atomic layer deposition (ALD) with tetrakisdimethylamino hafnium (TMAHf) as precursor. For all type of samples, post deposition annealing (PDA) at 400 °C in vacuum (10^{-8} Torr) for 30 min was implemented. In all cases the oxide thickness was measured by ellipsometry and TEM microscopy. Further details about the samples can be found in our previous works, Refs. 12–14.

Regarding the electrical measurements, the capacitors were subjected to constant voltage stresses (CVS) where the gate current was monitored as function of the time at different voltages using an Agilent Parameter Analyzer 4155C with a resolution in time of some milliseconds. In all cases, the measurements were performed at room temperature (300 K), and the bias was applied on the gate with the other terminal (wafer's back contact) grounded. Further details about the measurements of the BD transient can be found in Refs. 2–4.

In some cases, the CVS was periodically interrupted for Capacitance–Voltage (C–V) measurements to track the degradation of the device parameters such as the flat band voltage (V_{FB}).The C–V measurements were carried out using an Agilent 4285A LCR meter and the calculation of V_{FB} was performed by the recently introduced inflection point technique [15].

3. Results

3.1. Comparison between the initial degradation and the progressive breakdown regime

Fig. 1 shows typical BD transients observed under a constant voltage stress (CVS) with 100 mA current limit, for MOS stacks with different gate dielectrics, but similar metal gate (Ti/Au) and substrate (n-InGaAs). The layers (≈10 nm) of Al_2O_3, HfO_2, and Si_3N_4 correspond to Fig. 1(a), (b) and (c) respectively. At least two distinctive phases can be observed from all these curves shown in Fig. 1. The first part, which was extensively studied in [12], is characterized by a decrease of the current due to negative charge trapping, while the second part is characterized by a progressive increase of the current [16].Once the percolation path is completed by generation of defects within the dielectric layer, the BD event takes place and the gate current (I_G) changes trend and starts increasing [2–4,16]. It is a noisy and progressive process well in agreement with those reported in the literature for the cases of HfO_2 [4,17, 18] and SiO_2 [2–4,19]. The duration of the progressive increase of the current (dI_{BD}/dt) shows a strong voltage dependence (see inset in Fig. 3), and reach current levels of the order of 1–10 µA, where the gate current jumps abruptly to very high levels in times of the order of microseconds, i.e., limited by the bandwidth of the equipment. Note that the current level where the gate current jumps abruptly is on the same range for all cases with different CVS voltages. Therefore, as reported in our previous work [17], if the stress voltage is high enough to increase the background current above such level, only a fast runaway will be observed. In this framework, two relevant parameters can be defined as shown in Fig. 1(a).The time associated to the BD spot formation, named as the time-to-breakdown (t_{BD});and the period between the BD event and the jumps of the gate current to very high levels, named as the progressive BD time (t_{PBD}) [16,17].

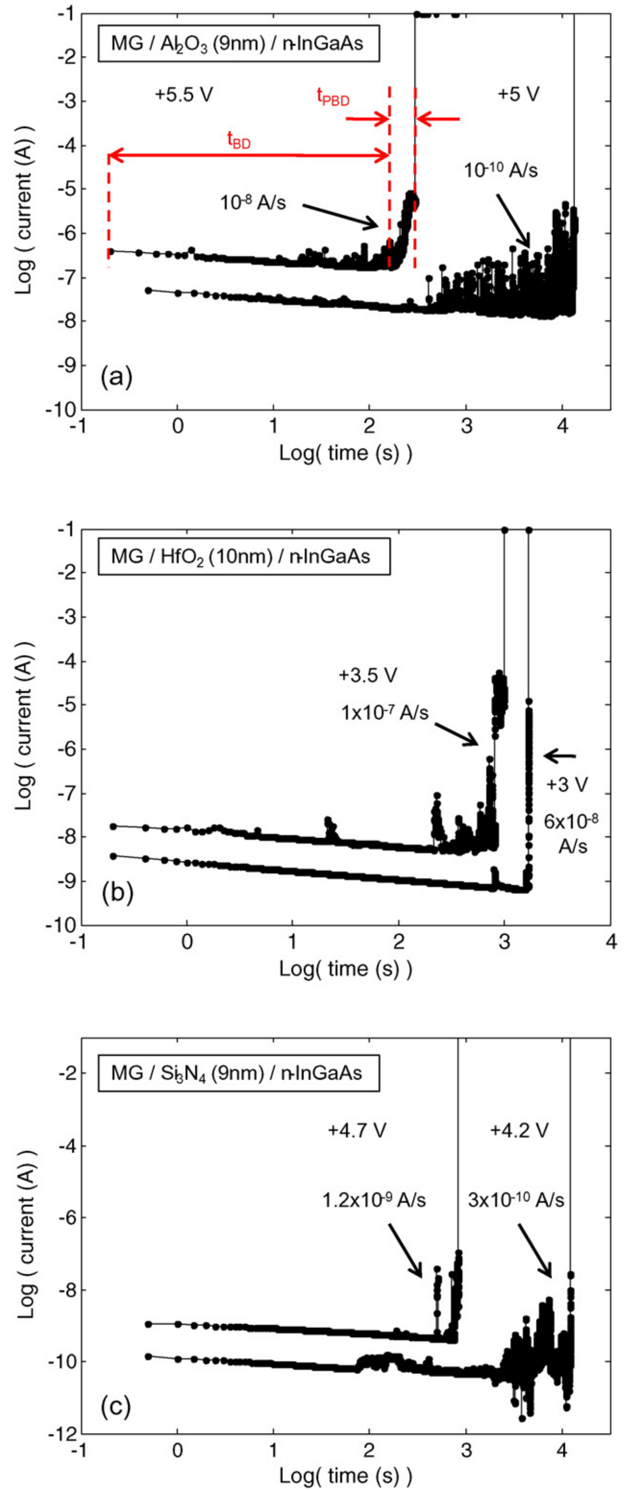

Fig. 1. Typical BD transients of gate current under constant voltage stress (CVS) for metal gate (MG)/Dielectric/InGaAs with a current compliance limit of 100 mA. The layers (≈10 nm) of Al_2O_3, HfO_2 and Si_3N_4 correspond to (a), (b) and (c) respectively.

Fig. 2(a) shows the evolution of t_{BD} (i.e. the first phase of the degradation) as function of the stress voltage ranging from +3 V to +6 V for all set of samples. Although it is not a statistical analysis, the large number of measurements is enough to show the main differences within each set [20]. For any value of stress voltage, it is observed that the set with Al_2O_3 layer shows the highest t_{BD}, while the set with HfO_2 layer

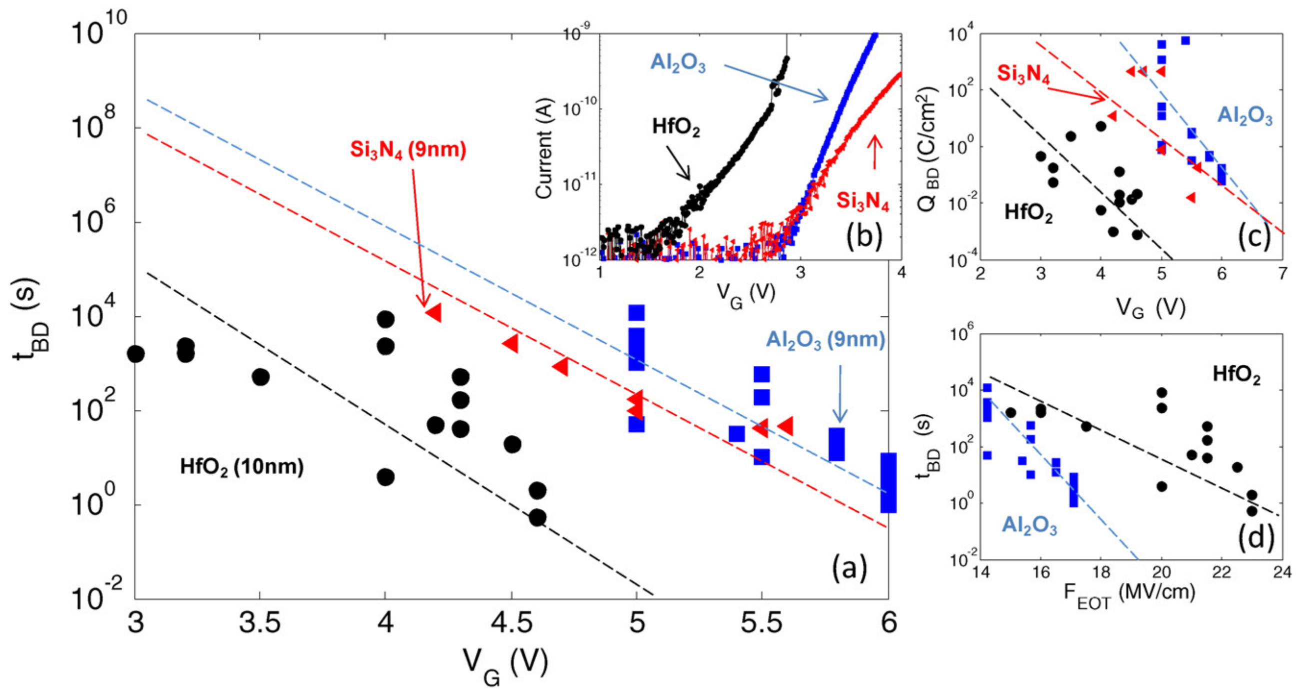

Fig. 2. Characteristics of the time-to-breakdown (t_{BD}) during CVS experiments for metal gate (MG)/Dielectric/InGaAs stacks in the case of 9 nm Al_2O_3 (square symbols), 10 nm HfO_2 (triangle symbols), and 9 nm Si_3N_4, (circle symbols) with a current compliance limit of 100 mA.(a) Correspond to t_{BD} vs. the stress voltage (V_G); (b) current–voltage characteristics (I–V) for all set of samples; (c)corresponds to the charge-to-breakdown (Q_{BD}) during the wear-out regime, as function of the stress voltage; and (d) correspond to t_{BD} vs. the electric field considering the t_{EOT} (equivalent oxide thickness).

shows lower values even though it is slightly thicker. Such a result may be due to the differences in the leakage current levels, due to variations in the semiconductor-oxide conduction band offsets. In particular, due to a smaller barrier for electron tunneling from the conduction band, the HfO_2 sample shows a higher leakage current level at low bias (see Fig. 2(b)), explaining the lower values of t_{BD} [20]. By studying the charge-to-breakdown (Q_{BD}) the same conclusion is obtained (see Fig. 2(c)).

Fig. 3 shows the t_{PBD} (i.e. the second phase of the degradation) as function of the stress voltage ranging from +3 V to +6 V for all set of samples of the previous figure. It is clear from the figure that the data from Al_2O_3 shows high values of t_{PBD}, and hence a slower progressive increase of the gate current, while for the HfO_2 layers faster breakdown growth rate with decreased t_{PBD} values in 5 orders of magnitude is observed. A strong dependence with voltage is observed in all cases [2, 4]. It is widely accepted that the evolution of the progressive BD current

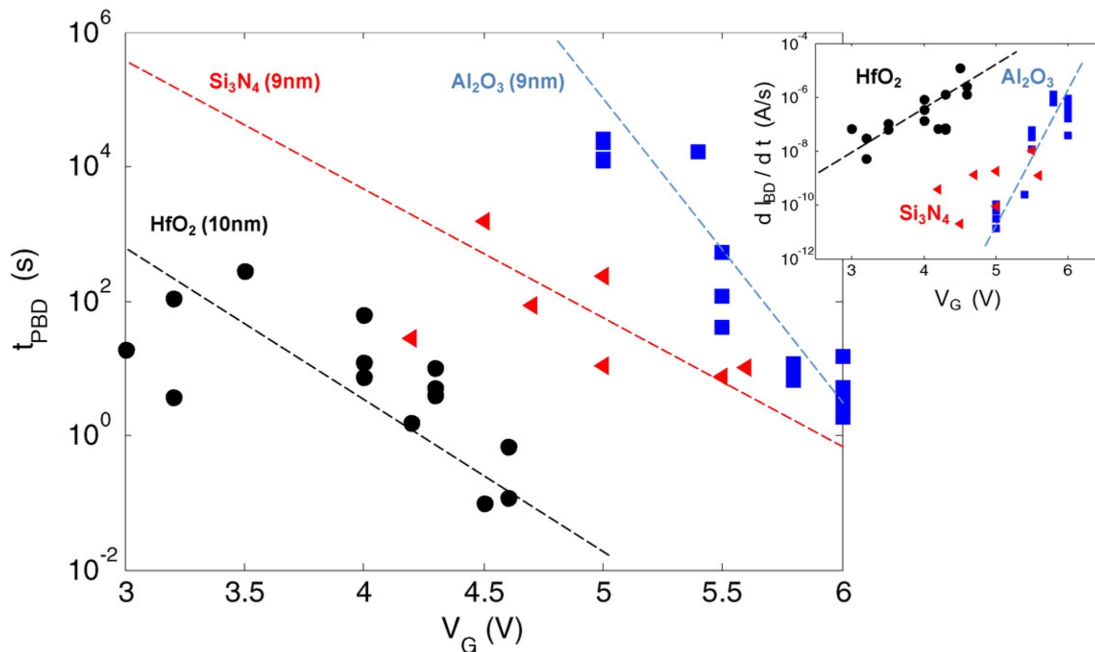

Fig. 3. Time duration of the progressive breakdown regime (t_{PBD}) as function of stress voltage (V_G) during CVS experiments for metal gate (MG)/Dielectric/InGaAs stacks in the case of 9 nm Al_2O_3 (square symbols), 10 nm HfO_2 (triangle symbols), and 9 nm Si_3N_4, (circle symbols). The inset corresponds to the degradation rate (dI_{BD}/dt) as function of the stress voltage for the same data.

may be quantified by the slope of the current during the BD event (t_{PBD}). For a better understanding, the inset of the Fig. 3 shows the dI_{BD}/dt values for different MOS stacks, of 1 nA to 10 μA. Although the leakage current levels are different with the samples for the studied bias range (see Fig. 2(b)), this analysis reflects the experimentally observed evolution of the current during the BD event. For example, in the case of Al_2O_3, the time to reach a current level of the order of 1 μA ranges from few seconds at +5.5 V, up to 10^{+4} s at + 5 V, while in the case of HfO_2 the time to reach a current level of the order of 1 μA ranges from a few seconds at +3.5 V, up to 10^{+3} s at +3 V. It is observed that the MOS stacks with high thermal conductivity (i.e Al_2O_3 and Si_3N_4) show similar dI_{BD}/dt (inset Fig. 3), while the duration of the breakdown transient decreases dramatically for HfO_2, even though the stress voltage is lower, and the oxide is slightly thicker. Table 1 shows the thermal conductivity of the studied samples.

Since a high-k/InGaAs interface with low density of defects is difficult to achieve and currently under intensive investigation [12–14], one may argue that a poor structural quality is the responsible of the results observed in Figs. 2(a) and 3, particularly in the case of the relatively fast BD observed for the HfO_2. The influence of the structural quality on the results will be discussed in detail in the next section.

Regarding the interpretation, the results of Fig. 3 can be explained by the thermal effect during the BD transient. It has been demonstrated that such a drastically different behavior among these various dielectric layers is due to the thermal conductivity of the oxide layers [16]. The breakdown growth rate during the second phase (named dI_{BD}/dt in the inset Fig. 3) is related to heat dissipation properties during the atomic diffusion of the cathode or anode atoms into the gate dielectric in the region of the percolation path [16].Therefore, dielectric layers with higher thermal conductivity will maintain the temperature of the percolation path below melting for longer times, and, hence showing smaller breakdown growth rates [16].This observation also states that the dI_{BD}/dt is an intrinsic characteristic of the dielectric layer, and it doesn't depend on the quality of the interfacial layer. In this regard, it is very important to compare our data measured on samples with InGaAs substrates with similar cases studied on samples with Si substrates. For example, the present case of the HfO_2 gate dielectric can be compared with [17], referring to the case of a TiN/HfO_2/interfacial SiO_2/Si substrate, with a 2.5 nm thick HfO_2 film and 1 nm SiO_2 layer. In this case, the dI_{BD}/dt values (about 10^{-8} to 10^{-10} A/s at 2.5–3 V)are similar to the values plotted in the inset of Fig. 3. According to our understanding reported in [16,21], it is indeed expected that dI_{BD}/dt depends on t_{ox}. Actually dI_{BD}/dt may also depend on the substrate, since electromigration may be different for Silicon vs. InGaAs (i.e. HfO_2 on Si different from HfO_2 on InGaAs). However, according to our model, such differences are expected to be minor as compared to the thermal conductivity of the dielectric layers. So in the present experiment, with a limited number of samples and with the statistical spread always observed in these cases, it is very difficult to put it in evidence, i.e., in a first approximation the dI_{BD}/dt values should be similar, as shown by the data of Fig. 3.

Fig. 4 shows the shift of V_{FB} (ΔV_{FB}) as function of the stress time for all set of samples at constant electric field (1 MV/cm).Since the recovery of trapped charge for the InGaAs/Al_2O_3 MOS system can be fast [22], special attention was taken to keep constant and small (100 ms) the

Table 1
Description of samples studied.

Dielectric	ε_{ox} [26]	Thermal conductivity [W/m.K] [27–31]	Melting temperature [K]	Substrate	Gate
Al_2O_3	~10	30	2300	InGaAs	Au
Si_3N_4	7	30	2100	InGaAs	Au
HfO_2	~20	1.1	3000	InGaAs	Au

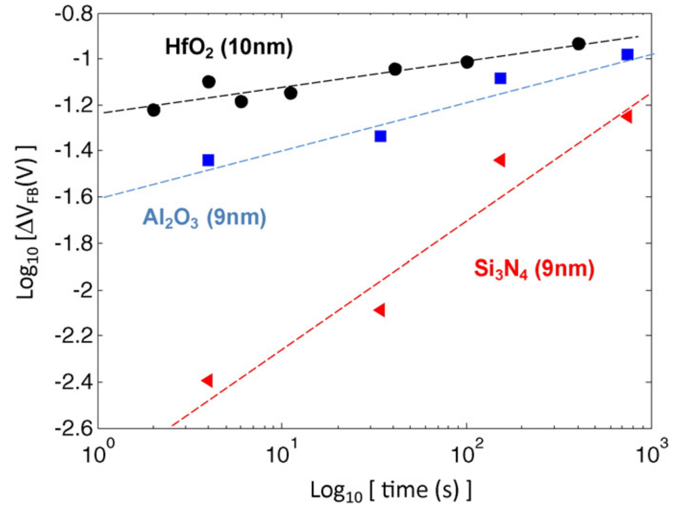

Fig. 4. Shift of the flat band voltage (ΔV_{FB}) as function of the time during CVS experiments at constant field (1 MV/cm).

values of the delay time between measurements. It is observed that the MOS stacks with Al_2O_3 and HfO_2 layers show similar degradation characteristics, while the Si_3N_4 shows a different behavior with a much lower V_{FB} shift.

The shift of V_{FB} can be attributed to charge trapping in the gate oxide. This interpretation is in a full correlation with the results in Fig. 1, where the gate current densities, measured at various stress voltages, decrease with the stressing time for all samples. Although it is not the topic of this work, the difference in the degradation rate between all samples may be due to different levels of leakage current [20] (see Fig. 2(b)). Although MOS stacks with Al_2O_3 and HfO_2 show similar degradation rates before the BD event(Fig. 4), there are differences between the values of t_{PBD} after the BD event(Fig. 3).The physical origin of such behavior may be due to different physical mechanisms in each phase. The initial degradation under CVS is controlled by the trapping effects on pre-existing and/or stress induced defects [4,12,20], while the progressive BD regime(i.e. after the BD event) is controlled by the heat dissipation properties during the atomic diffusion of the cathode or anode atoms into the gate dielectric in the region of the percolation path [16].

3.2. Influence of progressive breakdown on failure distribution

The failure distributions associated to both regimes (t_{BD} and t_{PBD}), named F_{BD} and F_{PBD}, are assumed to be Weibull distributions with different scale and shape parameters (t_{BD}, β_{BD}) and (t_{PBD}, β_{PBD}) respectively. The failure distribution for the first BD times (F_{BD})is well known to be a Weibull distribution [20], and F_{PBD} has been recently demonstrated to fit the Weibull model, particularly when the failure current is not too high as in our case [6].

The existence of the progressive BD in ultra-thin gate oxides had required an updating of the definition of the oxide failure; it has changed from the first jump in gate current to the leakage value that disrupts circuit operation [2,3,5]. In this context, the time to oxide failure (t_{FAIL}) is the sum of the time to BD (t_{BD}) and the residual time of the progressive increase of the current (t_{PBD})elapsed from the BD to the final failure (i.e. $t_{BD} + t_{PBD} = t_{FAIL}$). The distribution of interest for reliability is the cumulative distribution of the oxide failure (F_{FAIL}) and not that of the first BD (F_{BD}). It has been reported that the failure distributions considering the progressive BD, and hence associated to t_{FAIL} (i.e. F_{FAIL}) are non-Weibull distributions with a shallow region at high percentiles and a rapid decrease at low percentiles [6,9,10,11,23].Tours et al. [24] has proposed a compact model for F_{FAIL}, showed in Eq. (1), which is valid for any failure

percentile and for any combination of scale and shape parameters of each regime.

$$F_{FAIL}(t) = 1 - \exp\left\{-\left[\frac{\left(\frac{t}{\tau_{PBD}}\right)^{\beta_{PBD}}\left(\frac{t}{\tau_{BD}}\right)^{\beta_{BD}}}{\left(\frac{t}{\tau_{PBD}}\right)^{\beta_{PBD}} + \left(\frac{t}{\tau_{BD}}\right)^{\beta_{BD}}}\right]\right\} \quad (1)$$

This model, valid for single and multiple BD spots, reproduce very well the main aspect of the experimental data [24]. At high percentiles, F_{FAIL} converges toward the Weibull distribution of the first BD times, F_{BD}, whereas at low percentiles, it converges toward a Weibull distribution with a slope $\beta_{FAIL} = \beta_{BD} + \beta_{PBD}$ [10]. In this context, the first BD framework is only a special case with PBD time being negligibly small.

The model for F_{FAIL} (Eq. (1)) is a function of t_{PBD}/t_{BD} ratio and the shape parameters β's. In our case, the slopes (β_{BD} and β_{PBD}) for the F_{BD} and F_{PBD} distributions can be estimated from the experimental data. Although the number of measurements is small, it is enough to get a rough estimation of β_{BD} and β_{PBD}. In the case of Al_2O_3 at +6 V, β_{BD} and β_{PBD} are in the range of 2–3 and 2.5–3.5 respectively. Note that the values for the first BD times (β_{BD}) and progressive breakdown (β_{PBD}) are different corresponding to shallower slope at long times and steeper at short times. This is similar to the case of SiO_2 [3] and Al_2O_3 [25] with Si substrates, which also exhibits different β values. Since such β values correspond to a narrow statistical spread, it is possible to obtain a proper understanding of the failures distributions based on few measurements.

Based on such values of β_{BD} and $\beta_{PBD,}$ it is observed a strong dependence of F_{FAIL} with t_{PBD}/t_{BD} ($F_{FAIL}(t = 10\text{ s}) = 10^{-9}$ for $t_{PBD}/t_{BD} = 1$; $F_{FAIL}(t = 10\text{ s}) = 10^{-4}$ for $t_{PBD}/t_{BD} = 10^{-3}$), indicating large differences in failure distributions for different values of t_{PBD}/t_{BD}.

Fig. 5 shows the t_{PBD}/t_{BD} ratio as function of the stress voltage for each set of samples. It is observed that the MOS stacks with Al_2O_3 and Si_3N_4 layers have higher values than those with HfO_2 layers indicating the strong influence of the PBD regime. These results show that the bending of the failure distribution at low percentiles is not consequence to differences in the defect generation rate as suggested by others [7,8]. Fig. 4 shows that MOS stacks with Al_2O_3 and HfO_2 have similar degradation characteristics before BD, however the duration of the progressive increase such dielectric layers, t_{PBD}, is different by orders of magnitude (Fig. 3)generating different values of t_{PBD}/t_{BD}. The MOS stacks with Al_2O_3 and HfO_2 show $t_{PBD}/t_{BD} \geq 10^{-1}$ and $t_{PBD}/t_{BD} \leq 10^{-1}$ respectively,

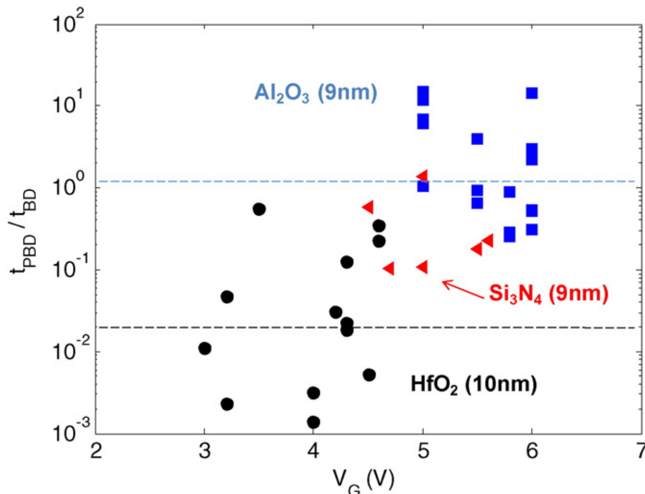

Fig. 5. Ratio of the duration of the progressive breakdown regime (t_{PBD}) and the time-to-breakdown (t_{BD}), marked as t_{PBD}/t_{BD}, as function of stress voltage (V_G) during CVS experiments for metal gate (MG)/Dielectric/InGaAs stacks in the case of 9 nm Al_2O_3 (square symbols), 10 nm HfO_2 (triangle symbols), and 9 nm Si_3N_4, (circle symbols) with a current compliance limit of 100 mA.

resulting in different distributions al low percentiles according to the model of Eq. (1) [24].

This observation is not an artifact due to a poor structural quality of the interfacial layer. The gate stack quality in terms of defects (i.e. interface states, border traps and leakage current) affects only the first phase of the current–time measurements, associated to the t_{BD} parameter. Since our data (see inset Fig. 3) show that the progressive BD regime is driven by thermal conductivity and not by the quality of the interfacial layer (IL), improving the IL will not affect the t_{PBD}.

Considering this observation, it is clear that these conclusions do not depend on the quality of the high-k dielectric layers. In particular, it is relevant for the HfO_2 that show the lower values of t_{BD}. In the hypothetic case of an increase of t_{BD} for HfO_2, it will not result in any change of the main results showed in Fig. 5 (i.e. ratio of t_{PBD}/t_{BD}), since an increase of t_{BD} for HfO_2 will only reinforce its differences with Al_2O_3 and Si_3N_4.

From the reliability point of view, even with a limited number of measurements as in our case, an ultimate comparison of the experimental data at similar field considering the equivalent oxide thickness (t_{EOT}) of each dielectric layer is useful. Fig. 2(d) shows the evolution of t_{BD} as function of F_{EOT} (electric field considering t_{EOT}) for the cases of Al_2O_3 and HfO_2 for a better understanding. Contrary to Fig. 2(a), it is observed that the set with HfO_2 layer shows the highest t_{BD} at similar F_{EOT}. However, though within the limits of a small statistics of samples, the Al_2O_3 shows a better trend by extrapolating to low fields.

In fact, the advantage of a higher thermal conductivity producing a longer progressive BD time for Al_2O_3 has to be weighted with respect to the disadvantage of the lower dielectric constant ($\varepsilon(Al_2O_3) < \varepsilon(HfO_2)$, see Table 1) which implies lower CMOS performance.

For reliability, as described above, the distribution of interest is the cumulative distribution of the oxide failure of t_{FAIL} (i.e. $t_{FAIL} = t_{BD} + t_{PBD}$). Fig. 6 shows the time to oxide failure (t_{FAIL}) — which is the sum of the time to BD (t_{BD}) and the residual time of the progressive increase of the current (t_{PBD}) elapsed from the BD to the final failure (i.e. $t_{BD} + t_{PBD} = t_{FAIL}$) — as function of the stress voltage ranging from +3 V to +6 V for all set of samples. It is observed that the t_{FAIL} of Al_2O_3 is many orders of magnitude higher than the rest, particularly than HfO_2. By considering the equivalent oxide thickness, however, the opposite conclusion is obtained, since the t_{FAIL} for Al_2O_3 is generally much lower, except for the case of low fields (see inset Fig. 6).

The occurrence of multiple competing BD events during the progressive BD event has been also a topic of debate during the last years. The results present in this work can contribute to a better understanding of this effect. In the simplest case, in which the t_{BD} lifetime is longer than the t_{PBD} time ($t_{PBD}/t_{BD} < 1$), t_{BD} is regarded as the first BD spot formation, and the PBD process represents growth of this BD spot. On the contrary, if the t_{BD} lifetime is shorter than the t_{PBD} time ($t_{PBD}/t_{BD} > 1$), it is claimed the occurrence of multiple BD spots before catastrophic BD based only on the difference between t_{PBD} and t_{BD} [9,11].The results presented in this paper suggest that a different interpretation is possible to model the dynamics of the BD of ultra-thin gate dielectrics in the case of the $t_{BD} \leq t_{PBD}$. The understanding of the physical mechanism involved that controls the progressive BD regime sets conditions of the occurrence of the multi-BD paths across the oxide.

As showed in Fig. 5, large ratio of t_{PBD}/t_{BD} ranging from 0.1 to 10 is only observed in dielectric layers with high thermal conductivity, as Al_2O_3 and Si_3N_4 (Table 1). As mentioned above, dielectrics with high thermal conductivity decrease the current growth rate (dI_{BD}/dt) in the progressive BD regime (t_{PBD}), since the heat dissipation in the vicinity of the BD spot maintains the temperature below the melting point of the dielectric for longer times. Therefore, one may consider the occurrence of just one BD spot if the thermal conductivity of the oxide layer is high enough. Moreover, as the leakage current increase during the PBD regime is limited by the increase of the temperature of the BD spot [16], the generation rate is heavily affected within the dielectric layer to form an additional percolation paths [4,20]. Further analysis of the microstructure changes are needed to confirm this observation.

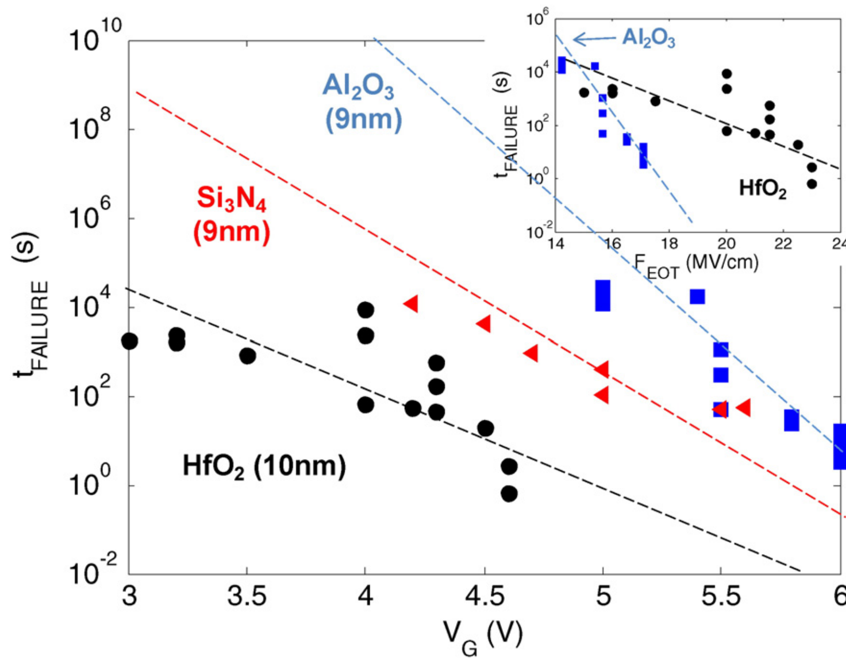

Fig. 6. Time to oxide failure (t_{FAIL}), which is the sum of the time to BD (t_{BD}) and the residual time of the progressive increase of the current (t_{PBD}) elapsed from the BD to the final failure (i.e. $t_{BD} + t_{PBD} = t_{FAIL}$) as function of stress voltage (V_G) during CVS experiments for metal gate (MG)/Dielectric/InGaAs stacks in the case of 9 nm Al_2O_3 (square symbols), 10 nm HfO_2 (triangle symbols), and 9 nm Si_3N_4, (circle symbols) with a current compliance limit of 100 mA. The inset corresponds to the same data as function of the electric field considering the t_{EOT} (equivalent oxide thickness).

4. Summary

In this work experimental data of BD transient of MOS stacks with different oxide layers (Al_2O_3, HfO_2 and Si_3N_4) have been studied in detail for InGaAs as substrate. The use of dielectric layers with different transient characteristics allowed a deep analysis of the influence of the progressive BD regime (t_{PBD}) in the failure distribution of the gate oxide.

Since the evolution of the BD spot, characterized by the progressive increase of the BD current, plays a major role for the reliability of MOS stacks, the failure distributions have been analyzed by the ratio between the progressive BD time and the first BD time (t_{PBD}/t_{BD}).It has been shown that the bending of failure distribution at low percentiles is exclusively attributed to the progressive BD regime.

The occurrence of multiple competing BD events during the progressive BD event has been also analyzed. The current flowing through the percolation path after the first BD event is entirely controlled by the heat dissipation in the vicinity of the percolation path toward the bulk of the dielectric layer. Hence, in dielectric layer with high thermal conductivity, as in our case, it occurs at a speed large enough to maintain the temperature of the percolation path below melting increasing the transient time during PBD regime. Under this conditions is reasonable assume that only one BD spot could be responsible of the failure of the device.

From the reliability point of view, the overall results show that Al_2O_3 presents better BD characteristics, since its high thermal conductivity provides a significant lifetime extension.

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References

[1] J.A. del Alamo, Nature 479 (2011) 310–316.
[2] B.P. Linder, S. Lombardo, J.H. Stathis, A. Vayshenker, D.J. Frank, IEEE Electron Device Lett. 23 (2002) 661–663.
[3] F. Monsieur, E. Vincent, D. Roy, S. Bruyere, J.C. Vildeuil, G. Pananakakis, G. Ghibaudo, IEEE Int. Rel. Phys. Symp. (2002) 45–54.
[4] S. Lombardo, J.H. Stathis, B.P. Linder, K.L. Pey, F. Palumbo, C.H. Tung, J. Appl. Phys. 98 (2005) 121301.
[5] B.P. Linder, J.H. Stathis, Microelectron. Eng. 72 (2004) 24–28.
[6] E. Wu, S. Tous, J. Suñé, IEDM Tech. Dig. (2007) 493–496.
[7] T. Nigam, A. Kerber, P. Peumans, IEEE Int. Rel. Phys. Symp. (2009) 523–530.
[8] G. Bersuker, N. Chowdhury, C. Young, D. Heh, D. Misra, R. Choi, IEEE Int. Rel. Phys. Symp. (2007) 49–54.
[9] E. Wu, J. Sune, B. Linder, R. Achanta, B. Li, S. Mittl, IEEE Int. Rel. Phys. Symp. (2011) (2A.1.1–2A.1.6).
[10] E. Wu, J. Suñé, IEEE Int. Rel. Phys. Symp. (2006) 54–62.
[11] S. Tsujikawa, M. Kanno, N. Nagashima, IEEE Trans. Electron Devices 58 (2011) 1468–1475.
[12] F. Palumbo, M. Eizenberg, J. Appl. Phys. 115 (2014) 014106.
[13] I. Krylov, A. Gavrilov, S. Cohen, D. Ritter, M. Eizenberg, ECS Trans. 41 (2011) 255–263.
[14] I. Krylov, A. Gavrilov, M. Eizenberg, D. Ritter, Appl. Phys. Lett. 101 (2012) 063504.
[15] R. Winter, J. Ahn, P.C. McIntyre, M. Eizenberg, J. Vac. Sci. Technol. B31 (2013) 030604.
[16] F. Palumbo, S. Lombardo, M. Eizenberg, J. Appl. Phys. 115 (2014) 224101.
[17] R. Pagano, S. Lombardo, F. Palumbo, P. Kirsch, S.A. Krishnan, C. Young, R. Choi, G. Bersuker, J.H. Stathis, Microelectron. Reliab. 48 (2008) 1759–1764.
[18] G. Condorelli, S. Lombardo, F. Palumbo, K.L. Pey, C.H. Tung, L.J. Tang, IEEE Trans. Device Mater. Reliab. 6 (2006) 534–541.
[19] F. Palumbo, S. Lombardo, J.H. Stathis, V. Narayanan, F.R. McFeely, J.J. Yurkas, IEEE Int. Rel. Phys. Symp. (2004) 122–125.
[20] J.H. Stathis, IBM J. Res. Dev. 46 (2002) 265–286.
[21] F. Palumbo, S. Lombardo, M. Eizenberg, IEEE Int. Rel. Phys. Symp. (2015) (5A.1.1–5A.1.6).
[22] J. Franco, A. Alian, B. Kaczer, D. Lin, T. Ivanov, A. Pourghaderi, K. Martens, Y. Mols, D. Zhou, N. Waldron, S. Sioncke, T. Kauerauf, N. Collaert, A. Thean, M. Heyns, G. Groeseneken, IEEE Int. Rel. Phys. Symp. (2014) (6A.2.1–6A.2.6).
[23] S. Sahhaf, R. Degraeve, P.J. Roussel, T. Kauerauf, B. Kaczer, G. Groeseneken, IEDM Tech. Dig. (2007) 501–504.

[24] S. Tous, E. Wu, J. Suñé, IEEE Electron Device Lett. 29 (2008) 949–951.
[25] T. Kauerauf, R. Degraeve, E. Cartier, C. Soens, G. Groesenenken, IEEE Electron Device Lett. 23 (2002) 215–217.
[26] H.-S.P. Wong, IBM J. Res. Dev. 46 (2002) 133–168.
[27] See www.nist.gov/srd/onlinelist.cfmfor NIST Standard Reference Database.
[28] M. Miyayama, K. Koumotoand, H. Yanagida, Engineering properties of single oxides, in: S.J. Schneider (Ed.), Engineered Materials Handbook, CRC Press, London 1991, pp. 748–749.
[29] S. Hampshire, in: S.J. Schneider (Ed.), Engineering Properties of Nitrides in Engineered Materials Handbook, CRC Press, London 1991, pp. 812–820.
[30] M.A. Panzer, M. Shandalov, J.A. Rowlette, Y. Oshima, W.-C. Yi, P.C. McIntyre, K.E. Goodson, IEEE Electron Device Lett. 30 (2009) 1269–1271.
[31] S.M. Sze, Physics of Semiconductor Devices, John Wiley & Sons, New York, 1981.